Low-Power System Design

Tuesday 20\textsuperscript{th} January 2009

Time: 14:00 – 16:00

Please answer THREE Questions from the FIVE questions provided

The use of electronic calculators is permitted provided they are not programmable and do not store text
1. **This question is concerned with the design of the ARM instruction set architecture.**

   a) Describe the register structure of an ARM processor, explaining any special roles of particular registers. (4 marks)

   b) Give an assembly language example of each of the following classes of ARM instruction, describing what the effect of your chosen instruction is:

   i) a data processing instruction; (2 marks)
   ii) a data transfer instruction; (2 marks)
   iii) a control flow instruction. (2 marks)

   c) The following ARM assembly code sequence prints out a text string:

   ```assembly
   TextOut     MOV     r0, #0x3
   NxtTxt      LDRB    r1, [r14], #1
   CMP         r1, #0
   SUBNE r1, r14, #1
   SWINE       SWI_ANGEL
   BNE         NxtTxt
   ADD         r14, r14, #3
   BIC         r14, r14, #3
   MOV         pc, r14
   END
   ```

   Write a short assembly program that illustrates how this routine is called. (4 marks)

   d) Explain the operation and role of the following instructions in the above code:

   i) the 'LDRB' in the 2\textsuperscript{nd} instruction (2 marks)
   ii) the 'SWINE' in the 5\textsuperscript{th} instruction (2 marks)
   iii) the 'BIC' in the 8\textsuperscript{th} instruction (2 marks)
2. **This question is concerned with using the Thumb architecture in low-power system design.**

   a) What is the role of the Thumb instruction set in low-power embedded system designs based around the ARM7TDMI? (2 marks)

   b) Assuming that a Thumb program is typically 70% of the size of the equivalent ARM program, estimate the relative performance of the Thumb and ARM programs when both are running from either:

      i) zero wait-state 32-bit on-chip RAM, or (4 marks)
      ii) slow 16-bit off-chip memory. (4 marks)

   In a particular complex low-power application based around a 20 MHz ARM7TDMI core, some speed critical routines are held in zero wait-state 32-bit on-chip RAM while the rest of the software runs from 100 ns 16-bit off-chip memory.

   c) Describe a procedure based on the ARM toolkit for identifying the routines which should be run from on-chip memory. (3 marks)

   d) What are the performance and power-efficiency benefits of the on-chip memory? (Quantify where you can.) (4 marks)

   e) What are the power-efficiency benefits of using Thumb code in the off-chip memory? (3 marks)

3. **This question is concerned with the design of low-power cache memories.**

   a) Describe the role of a cache in a low-power embedded system. (4 marks)

   b) Sketch the organizations of each of the following caches:

      i) direct-mapped; (3 marks)
      ii) 2-way set associative; (3 marks)
      iii) fully associative. (3 marks)

   c) What are the issues that must be taken into account when selecting a cache organization for a low-power system? (4 marks)

   d) Describe techniques that can be used to reduce cache power consumption. (3 marks)
4. **This question is concerned with microprocessor pipelines.**

   a) What is the role of a pipeline in a processor organization? (2 marks)

   b) Describe the basic 3-stage pipeline used in the ARM6/ARM7 and compare and contrast it with the 5-stage pipeline used in StrongARM and ARM9TDMI. Why is the 5-stage pipeline faster and why is it substantially more complex than the 3-stage pipeline? (8 marks)

   The StrongARM has a dedicated branch adder in the decode stage of its pipeline, whereas ARM9TDMI computes branch target addresses in its main ALU.

   c) What is the saving in branch latency resulting from the dedicated branch adder? Explain your answer. (3 marks)

   d) What is the impact on performance of the dedicated branch adder? (You may assume that both processors have an average CPI around 1.2 and that taken branches account for 20% of a typical instruction mix.) (7 marks)

5. **This question is concerned with the system development process.**

   a) In which order might each of the following technologies be used in a typical system development project, and what role would each play?

      i) on-chip debug support, such as EmbeddedICE (3 marks)
      ii) on-chip macrocell buses, such as AMBA (3 marks)
      iii) software system modelling, using (for example) the ARMulator (3 marks)

   b) Sketch a suitable system-on-chip organisation for the following macrocells: an ARM9TDMI core with instruction and data caches; a DMA controller; a 32 Kbyte ROM; an external memory interface; a UART; a parallel interface. (The system should use both ASB and APB buses appropriately.) (7 marks)

   c) What are the problems associated with obtaining a real-time trace of processor activity in a complex System-on-Chip, and what solutions may be employed to overcome these problems? (4 marks)

**END OF EXAMINATION**