Low-Power System Design

Date: Tuesday 19th January 2010

Time: 14.00 – 16.00

Please answer THREE Questions from the FIVE questions provided

The use of electronic calculators is permitted provided they are not programmable and do not store text
1. **This question is concerned with the design of the ARM instruction set architecture.**

   a) The ARM processor uses a ‘load-store’ architecture. Explain what this means in terms of the instruction set architecture, and give an example of an instruction that would **not** be included in a load-store architecture. (4 marks)

   b) Draft ARM code to add two 32-bit values held in memory and store the result in a third memory location. (2 marks)

   c) Write an efficient ARM assembly program that copies a 1Kbyte block of values from one location in memory to another non-overlapping 1Kbyte area. You may assume that both source and destination areas start at word-aligned addresses. (6 marks)

   d) Outline briefly how your code in c) would have to be changed in each of the following circumstances:

      i) the two 1Kbyte areas overlap, with the source starting at a higher address location than the destination; (2 marks)

      ii) the two 1Kbyte areas overlap, with the source starting at a lower address than the destination; (2 marks)

      iii) the source and destination start at arbitrary (non-word-aligned) byte addresses. (4 marks)
2. This question is concerned with using the Thumb architecture in low-power system design.

   a) Assuming that a Thumb program is typically 70% of the size of the equivalent ARM program, estimate the relative performance of the Thumb and ARM programs when both are running from either:

      i) zero wait-state 32-bit on-chip RAM, or                     (4 marks)
      ii) slow 16-bit off-chip memory.                             (4 marks)

   In a particular complex low-power application based around a 20 MHz ARM7TDMI core, some speed critical routines are held in zero wait-state 32-bit on-chip RAM while the rest of the software runs from 100 ns 16-bit off-chip memory.

   b) Describe a procedure based on the ARM toolkit for identifying the routines which take the majority of the execution time.                             (4 marks)

   c) Hence discuss strategies for deciding where to locate each routine and whether to compile each routine into ARM or Thumb code.                     (8 marks)

3. This question is concerned with the design of system memory hierarchies for low-power applications.

   a) Why is the organisation of on-chip memory critical in the design of a low-power system?                      (3 marks)

   b) On-chip memory may be organised as simple memory-mapped RAM or as a cache. Discuss the principal advantages and drawbacks of each of these organisations.     (5 marks)

   An ARM processor employs a cache that uses a content-addressable memory (CAM) tag store with one tag for every word of data, but it is found that the tag store consumes too much power.

   c) Sketch the organisation of the cache.                                                                 (2 marks)

   d) Suggest three modifications to the cache that should reduce its power consumption considerably whilst retaining its highly associative operation.        (6 marks)

   e) Estimate the power-savings that each of these modifications should yield.                                (4 marks)

   [PTO]
4. This question is concerned with microprocessor pipelines.
   a) What is the role of a pipeline in a processor organization? (2 marks)
   b) Describe the basic 3-stage pipeline used in the ARM6/ARM7 and sketch pipeline timing diagrams showing:
      i) the execution of consecutive data processing instructions; (4 marks)
      ii) a series of data processing instructions before and after one data store instruction; (4 marks)
      iii) a series of data processing instructions before and after a branch instruction. (4 marks)
   c) Estimate the CPI of a 3-stage pipeline ARM processor on the assumption that a typical instruction mix is 20% taken branches, 40% single data transfer instructions and 40% data processing instructions. (6 marks)

5. This question is concerned with the system development process.
   a) Describe each of the following technologies which are to be used in a typical system development project, say whether each would be used by the chip designer, the system architect or the software developer, and suggest what it would be used for.
      i) on-chip debug support, such as EmbeddedICE (3 marks)
      ii) on-chip macrocell buses, such as AMBA (3 marks)
      iii) software system modelling, using (for example) the ARMulator (3 marks)
   b) Sketch a suitable system-on-chip organisation for the following macrocells: an ARM7TDMI core; a DMA controller; a 32 Kbyte ROM; a 32 Kbyte RAM; an external memory interface; a UART; a parallel interface. (The system should use both ASB and APB buses appropriately.) (7 marks)
   c) How might the external memory interface be extended to facilitate chip production test? (4 marks)

END OF EXAMINATION