Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Mobile Systems

Date:   Monday 17th January 2011
Time:   09:45 - 11:45

Please answer any THREE questions from the FIVE questions provided

For full marks your answers should be concise as well as accurate. Marks will be awarded for reasoning and method as well as being correct.

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text.

[PTO]
1. **This question is concerned with the design of the ARM instruction set.**

   a) The design of the ARM instruction set was greatly influenced by the RISC (Reduced Instruction Set Computer) ideas being put forward at the time of its development. Which of the following aspects of the ARM architecture are characteristic features of RISC processors, and which are more specific to the ARM?

   (In each case give a sentence explaining what the feature is and say whether it is a general RISC characteristic or specific to the ARM. Where appropriate, give an example.)

   i) a load-store architecture
   ii) conditional execution of all instructions
   iii) combined shift and add instructions
   iv) a large, regular register file
   v) support for a 2nd compressed instruction set
   vi) fixed-length instruction encoding
   vii) single instructions that load or store many registers
   viii) auto-indexed addressing modes
   ix) single cycle execution of (some) instructions
   x) banked registers for exception handling.  

   The following ARM assembly code sequence could be generated by a compiler: ('...' indicates further instructions or constants)

   ```assembly
   ADR   r1, TABLE
   CMP   r0, #TABLEMAX
   LDRLS pc, [r1,r0,LSL #2]
   ... ; statementsD
   B    EXIT
   TABLE DCD L0
   DCD  L1
   ...
   DCD  LN
   L0   ... ; statements0
   B    EXIT
   L1   ... ; statements1
   B    EXIT
   ...
   LN   ... ; statementsN
   EXIT ...
   ```

   b) What C source code could this assembly code represent?  

   Explain the role of the following aspects of the code:

   i) the 'ADR' in the 1st instruction
   ii) the 'LS' in the 3rd instruction
   iii) the 'LSL' in the 3rd instruction

   (4 marks)

   (2 marks)

   (2 marks)

   (2 marks)
2. **This question is concerned with the use of 'Thumb' code in low-power applications and its implementation in ARM processor cores.**

   a) What was the principal motivation for the introduction of Thumb code into ARM processors? (3 marks)

   b) Describe the mechanisms employed in the ARM7TDMI and ARM9TDMI to support Thumb code, highlighting and explaining any differences between how the two processors provide this support. (5 marks)

   c) Describe the way Thumb code is developed in a typical small embedded system and how the system designer achieves optimum cost and power-efficiency whilst meeting critical real-time performance requirements. (12 marks)

3. **This question is concerned with the design of system memory hierarchies for low-power applications.**

   a) Why is the organisation of on-chip memory critical in the design of a low-power system? (3 marks)

   b) On-chip memory may be organised as simple memory-mapped RAM or as a cache. Discuss the principal advantages and drawbacks of each of these organisations. (5 marks)

   An ARM processor employs a cache that uses a content-addressable memory (CAM) tag store with one tag for every word of data, but it is found that the tag store consumes too much power.

   c) Sketch the organisation of the cache. (2 marks)

   d) Suggest three modifications to the cache that should reduce its power consumption considerably whilst retaining its highly associative operation. (6 marks)

   e) Estimate the power-savings that each of these modifications should yield. (4 marks)
4. This question is concerned with the design of memory management systems.

Outline the operation of:

a) a segmented memory management system (5 marks)
b) a two-level page table (5 marks)

(In each case sketch the organisation of the system and show how a processor address is translated.)

c) What is the role of a translation look-aside buffer (TLB)? (2 marks)

d) Estimate the improvement in performance that would result from adding a TLB to a processor system (with no cache memory) that employs a two-level page table. Assume that the TLB has a 98% hit rate. State any other assumptions that you make. (8 marks)

5. This question is concerned with the system development process.

a) Give brief descriptions of the following technologies and their roles in system development:
   
i) on-chip debug support, such as EmbeddedIce (3 marks)
   ii) on-chip macrocell buses, such as AMBA (3 marks)
   iii) software system modelling, using (for example) the ARMulator (3 marks)

b) Sketch a suitable system-on-chip organisation for the following macrocells: an ARM7TDMI core; a DMA controller; a 4 Kbyte RAM; a 16 Kbyte ROM; an external memory interface; a UART; a parallel interface. (The system should use both ASB and APB buses appropriately.) (7 marks)

c) Describe how the bus system can assist in production testing of the finished chip. (4 marks)

END OF EXAMINATION