Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Mobile Systems

Date: Thursday 19th January 2012
Time: 09:45 - 11:45

Please answer any THREE questions from the FIVE questions provided

For full marks your answers should be concise as well as accurate. Marks will be awarded for reasoning and method as well as being correct.

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text.

[PTO]
1. This question is concerned with the design of the ARM instruction set.

a) What are the principal characteristics of a Reduced Instruction Set Computer (RISC)? (4 marks)

b) Discuss the extent to which the ARM architecture adopts RISC characteristics, and list three ARM features that are not characteristic of other RISC processors. (5 marks)

c) The following ARM assembly code sequence is a subroutine that computes the greatest common divisor of two positive integers (the largest integer that divides exactly into each number):

```
GCD  CMP  r0, r1
SUBLT r1, r1, r0
SUBGT r0, r0, r1
BNE  GCD
MOV  PC, r14
```

If on entry to the subroutine $r0 = 49$ and $r1 = 35$, describe the sequence of register values that leads to a result being returned. (4 marks)

d) Show how the above code would have to be modified if ARM did not support conditional execution of all instructions but only supported conditional branches. (5 marks)

e) For this example, how much benefit does conditional execution deliver in terms of code size and the energy required to execute the subroutine? (2 marks)
2. **This question is concerned with the use of 'Thumb' code in low-power applications and its implementation in ARM processor cores.**

   a) What is Thumb code, and why was it introduced into the ARM instruction set architecture?  
      (3 marks)

   b) The Thumb instruction set can be implemented by decoding Thumb instructions into the corresponding 32-bit ARM instructions, or by directly decoding the datapath controls from the Thumb instruction. What are the advantages and disadvantages of each approach?  
      (5 marks)

   c) Describe the development of a small embedded application with real-time constraints that uses ARM-Thumb interworking to achieve the optimum balance of performance and memory requirements.  
      (12 marks)

3. **This question is concerned with the design of cache memories for low-power applications.**

   a) An ARM processor employs a 32 Kbyte associative cache that uses a content-addressable memory (CAM) tag store with one tag for every word of data. Sketch the organization of the cache, being careful to indicate exactly how all address lines are used to access data in the cache.  
      (5 marks)

   b) The cache is found to consume too much power so the organization is modified to increase the cache line-length to 4 words. Again, sketch the organization of the cache.  
      (5 marks)

   c) The cache still consumes too much power. The organization is further modified to reduce the associativity by splitting the CAM into 4 sections. Again, sketch the organization of the cache.  
      (5 marks)

   d) Explain why each of the above steps might be expected to reduce the power used by the cache, and in each case by how much.  
      (3 marks)

   e) Suggest a further way of reducing the cache power, still using the basic organization in c).  
      (2 marks)
4. This question is concerned with the design of memory management systems.
   a) Describe the principles of operation of a 2-level paged Memory Management Unit (MMU), and sketch its operation. (5 marks)
   b) Describe the principles of operation of a Memory Protection Unit (MPU), and sketch its organization. (5 marks)
   c) Where might you expect to find an MMU used, and where might you expect to find an MPU used? (2 marks)
   d) Estimate the improvement in performance that would result from adding a Translation Look-aside Buffer (TLB) to a processor system (with no cache memory) that employs a two-level page table MMU. Assume that the TLB has a 99% hit rate. State any other assumptions that you make. (8 marks)

5. This question is concerned with the system development process.
   a) What is In-Circuit Emulation (ICE), and why is it a problem for designs that use System-on-Chip (SoC) technology? (5 marks)
   b) Describe the facilities provided in ARM’s Embedded-ICE on-chip debug technology, and discuss the extent to which they support the functionality expected in an ICE system. (5 marks)
   c) Sketch the interconnect scheme used by the ARM Advanced High-performance Bus (AHB) to connect 4 master clients to 2 slave clients. Take particular care to show how the address, write data and read data buses are connected. (7 marks)
   d) What is the role of the arbiter in AHB interconnect? (3 marks)

END OF EXAMINATION