Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

M.Sc. in Advanced Computer Science

System Level Design

Date: Friday 16th May 2008

Time: 09:45 – 11:45

Please answer any THREE Questions from the FIVE questions provided

This is a CLOSED book examination

The use of electronic calculators is NOT permitted
Figure 1: Untimed Transaction Level Model

Figure 1 shows a diagram of the untimed Transaction Level Model of a drawing system that you have been using in the coursework.
1. a) Explain the principles underlying a Transaction Level Model (TLM) for System-on-Chip design and the advantages of this approach. (5 marks)

b) Does using a TLM have disadvantages and if so what? (2 marks)

c) Explain how the Inquisitor aids testability of the system and describe how a command to read a byte from the frame store is assembled and executed via the Inquisitor. (7 marks)

d) If a new module to draw another shape is added to the system, indicate what changes would need to be made to the untimed TLM of Figure 1 in order to accommodate it. (2 marks)

e) Computation blocks and channels can be timed or untimed leading to exploration of different facets of the design in a TLM. For each of the following cases say what exploration would be possible:

   i) computation blocks untimed, channels untimed
   ii) computation blocks untimed, channels timed
   iii) computation blocks timed, channels untimed
   iv) computation blocks timed, channels timed. (4 marks)

2. a) Identify the master(s) and slave(s) connected to the Video Channel in Figure 1 and hence explain the need for arbitration in the Video Channel in a timed Transaction Level Model. (4 marks)

b) Explain how arbitration is implemented in the Video Channel of the timed Transaction Level Model. (3 marks)

c) If the frame store is 32 bits wide and has an access time of 55 nsecs, the screen needs 4 bytes every 160 nsecs and the Video Channel clock period is 20 nsecs, show that the screen can be serviced at an adequate rate. Aid your answer with a timing diagram showing the servicing of read requests from the CRT controller. (5 marks)

d) Explain whether the screen would be serviced properly if:

   i) the Video Channel clock period was 10 nsecs
   ii) the Video Channel clock period was 40 nsecs
   iii) the Video Channel clock period remained 20 nsecs but the frame store width was reduced to 16 bits. (8 marks)

[PTO]
3. Program 1 shows “process Transaction”, a method associated with the Video Channel, in Figure 2.

a) Explain the purpose of this code and how it is achieved. (6 marks)

b) Explain what type of SystemC feature is “proceed” and what is it used for in the code? (4 marks)

c) With what type of SystemC process (SC_METHOD or SC_THREAD) would you instantiate this code? Explain why. (4 marks)

d) Show, using SystemC or pseudo code, how you would modify the code to give all requestors fair access to the channel. (6 marks)

```c
void VideoChannel::processTransactions() {
    while (true) {
        /* suspend until next positive edge of the clock */
        wait(clk.posedge_event());
        /* priorities are fixed in this model */
        if (requestIn[CRTC_ID]) {
            /* process CRT controller transaction */
            /* give the go ahead */
            proceed[CRTC_ID].notify();
            /* and wait for completion */
            wait(completed);
        }
        else if (requestIn[DE_ID]) {
            /* process drawing engine controller transaction */
            /* give the go ahead */
            proceed[DE_ID].notify();
            /* and wait for completion */
            wait(completed);
        }
        else if (requestIn[IQ_ID]) {
            /* process inquisitor controller transaction */
            /* give the go ahead */
            proceed[IQ_ID].notify();
            /* and wait for completion */
            wait(completed);
        }
    }
}
```

PROGRAM 1

Figure 2
4. a) With the aid of a diagram of the design hierarchy for System-on-Chip design, briefly describe the stages in moving from a system specification to implementation. (8 marks)

b) The gap between the numbers of devices on a chip and person productivity is widening. Discuss how this might be addressed through the use of:

i) application specific standard parts (ASSPs)
ii) reconfigurable computing
iii) chip multiprocessors
iv) IP blocks

What are the advantages and disadvantages of each of these approaches? (12 marks)

5. a) In timed models of the drawing system, the modules to the left of the dotted line operate from one clock (mclk) and those to the right from another clock (vclk). Explain the synchronisation that needs to take place in crossing from one clock domain to another:

i) in the timed Transaction Level Model
ii) in the Register Transfer Level (RTL) design.

Aid your description at the RTL by drawing the logic required. (8 marks)

b) At the RTL level, modules to the right communicate using handshake signals. Explain what is meant by this and give a timing diagram showing the transfer of:

i) a write request
ii) a read request (7 marks)

c) Discuss how the RTL simulation of the drawing machine can be debugged. (5 marks)

END OF EXAMINATION