Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Mobile Systems

Date: Thursday 16th May 2013
Time: 14:00 - 16:00

Please answer any THREE Questions from the FIVE Questions provided

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text.

[PTO]
1. **This question is concerned with the design of the ARM instruction set.**

   a) What is a load-store architecture?  
      (2 marks)

   b) In the context of the ARM architecture, what is meant by conditional execution?  
      (2 marks)

   c) Give an example of how an if… then… else… C statement might be compiled into ARM instructions with and without the use of conditional execution (conditional branches being allowed in both cases).  
      (5 marks)

   d) Describe what happens when an ARM processor receives an IRQ interrupt request. Be clear about what determines whether the interrupt request has any effect, when it takes effect, and what effect it has on program execution.  
      (5 marks)

   e) What must the interrupt service routine do to ensure that the user program can resume as if nothing had happened once the interrupt has been serviced?  
      (3 marks)

   f) What more must the interrupt service routine do to allow re-entrant interrupt handling (i.e. another interrupt to be serviced during this service routine)?  
      (3 marks)

2. **This question is concerned with the use of 'Thumb' code in low-power applications and its implementation in ARM processor cores.**

   ARM processors such as the ARM7TDMI can execute two instruction sets: standard 32-bit ARM instructions, and 16-bit Thumb instructions.

   a) What is the relationship between Thumb and ARM code that limits the choice of instructions that could be included in the Thumb instruction set?  
      (3 marks)

   b) How is Thumb implemented in the ARM7TDMI?  
      (3 marks)

   c) How is Thumb implemented in the ARM9TDMI? Explain why this differs from the ARM7TDMI implementation, and why this difference was necessary.  
      (4 marks)

   d) Thumb code typically occupies 30% less memory than the equivalent ARM code. Why is it not 50% smaller?  
      (2 marks)

   e) What does this size relationship mean for the performance and power-efficiency of an ARM7TDMI-based system? Discuss this in the context of various typical memory subsystems.  
      (8 marks)
3. This question is concerned with the design of cache memories for low-power applications.

   a) An ARM processor employs a 32 Kbyte direct-mapped cache that uses a RAM tag store with one tag for every word of data. Sketch the organization of the cache, being careful to indicate exactly how all address lines are used to access data in the cache, and remembering that ARM uses byte addresses! (10 marks)

   b) The cache is found to consume too much power so the organization is modified to increase the cache line-length to 4 words. Again, sketch the organization of the cache. (5 marks)

   c) The cache is then found to have too poor a hit rate, so it is decided to modify it to 2-way set associative. Without a detailed diagram, describe briefly how the organisation changes and how the various memory dimensions (such as the width of the RAM tag store) change. (5 marks)

4. This question is concerned with the design of memory management systems.

   a) Sketch the organisation of a 2-level paged Memory Management Unit (MMU), showing how the various fields in the processor’s logical address are used in the translation process. (5 marks)

   b) How may memory protection mechanisms be incorporated into an MMU, and what functionality do they offer? (5 marks)

   c) If address translation is not required, but some form of memory protection is still required, how may this be implemented? (3 marks)

   d) Estimate the improvement in performance that would result from adding a Translation Look-aside Buffer (TLB) to a processor system (with no cache memory) that employs a two-level page table MMU. Assume that the TLB has a 98% hit rate. State any other assumptions that you make. (7 marks)
5. **This question is concerned with the system development process.**

a) In which order might each of the following technologies be used in a typical system development project, and what role would each play?

i) on-chip debug support, such as EmbeddedIce (3 marks)

ii) on-chip macrocell buses, such as AMBA (3 marks)

iii) software system modelling, using (for example) the ARMulator (3 marks)

b) Sketch a suitable system-on-chip organisation for the following macrocells: an ARM9TDMI core with instruction and data caches; a DMA controller; a 32 Kbyte ROM; an external memory interface; a UART; a parallel interface. (The system should use both ASB and APB buses appropriately.) (7 marks)

c) What are the problems associated with obtaining a real-time trace of processor activity in a complex System-on-Chip, and what solutions may be employed to overcome these problems? (4 marks)

END OF EXAMINATION