Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Mobile Systems

Date: Thursday 22nd May 2014
Time: 14:00 - 16:00

Please answer ALL Questions

This is a CLOSED book examination

The use of electronic calculators is NOT permitted

[PTO]
1. Questions concerning the ARM architecture

   a) What is a load-store architecture?
   What are the main characteristics of a load-store architecture? (2 marks)

   b) The ARM architecture provides very good code density.
   Let us consider the following arithmetic instruction:
   \[
   \text{ADD } r1, r2, r3
   \]
   What additional operation(s) can the ARM architecture provide together with a data
   processing instruction?
   Give for each operation(s) a use case where this improves code density. (4 marks)

   c) ARM processors such as the ARM7TDMI can execute two instruction sets:
   standard-32bit ARM instructions and 16-bit Thumb instructions.
   Discuss the main factors that impact code size, processor performance and processor
   power consumption when using Thumb instructions instead of standard 32-bit ARM
   instructions. (4 marks)

   d) Discuss the impact of Thumb instructions instead of standard 32-bit ARM
   instructions on performance and power when considering different
   (hierarchical) memory subsystems. (4 marks)

   e) ARM supports interrupts (IRQ) and fast interrupts (FIQ).
   What makes FIQs faster than IRQs? (3 marks)

   f) Many mobile systems have multicore CPUs.
   Why does this help reducing power consumption? (3 marks)
2. Questions concerning programming the ARM architecture

a) The following code from the first exercise prints ‘Hello World’ on the screen:

```assembly
ENTRY ;code entry point
ADR  r1, TEXT-1 ;r1->‘Hello World’
MOV  r0, #0x3 ;select Angel SYS_WRITEC
LOOP LDRB r2, [r1,#1]! ;get next byte
    CMP r2, #0 ;check for text end
    SWINE SWI_ANGEL ;if not end print...
    BNE LOOP ;..and loop back
Exit ;end of execution
ALIGN ;to ensure ADR works
TEXT DATA
    = 'Hello World',&a,&d,0
END ;end of program source
```

The program initializes `r1` with `TEXT-1`. What do you have to change when initializing `r1` with `TEXT (ADR r1, TEXT)`? (4 marks)

Do not simply decrement `r1` before entering the loop!

What is the difference in performance? (4 marks)

b) Describe what happens when an ARM processor receives a software interrupt (SWI). Assume that the processor is running in user mode with no interrupts masked. (4 marks)

c) Considering the last question, after just entering the SWI handler, what happens and how is it processed when an ARM processor receives:

i) a normal interrupt (IRQ)? (2 marks)

ii) a fast interrupt (FIQ)? (2 marks)

d) What must a SWI (SWI_A) do when calling a nested SWI (SWI_B) from within SWI_A? (3 marks)

e) Describe briefly what it means when subroutines adhere to the APCS (ARM Procedure Call Standard). (5 marks)
3. Questions about memory

a) The two main approaches for memory management are segmentation and paging.

i) Why is memory management useful for allowing multiple active programs? (2 marks)

ii) What is the difference between a logical address (sometimes called virtual address) and a physical address? (You do not have to discuss issues related to caches at this point.) (2 marks)

iii) Describe the basic principles behind segmentation and paging. How are physical addresses created and protected in each variant? (You can draw figures and/or use text for answering this question.) Discuss the main advantages and disadvantages of each variant. (8 marks)

b) Most systems use a DRAM variant as the main memory. DRAM arranges data in an array of memory cells which is accessed by a row access select (RAS) and by a column access select (CAS).

i) What is the difference on power and performance when
   1) incrementally changing row access and
   2) incrementally changing col access? (2 marks)

ii) Consider you have to connect a DRAM to a CPU. How would you allocate address signals for row select and for column select? Please justify your decision. (2 marks)

c) In some embedded systems, on-chip RAM is used in preference to a cache. Give the most important reasons for this. (2 marks)

d) What can be changed in the cache organization to increase the hit rate without making the cache memory size larger? How does this impact implementation cost? (2 marks)