Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Mobile Systems

Date: Monday 1st June 2015
Time: 09:45 - 11:45

Please answer ALL Questions

This is a CLOSED book examination

The use of electronic calculators is NOT permitted

[PTO]
1. Questions concerning the ARM architecture

   a) How does ARM increments the content of a value stored somewhere in memory?  
      (2 marks)

   b) What restrictions or changes have been made to make Thumb code more compact
      than code that is running in standard 32-bit ARM mode?  
      (3 marks)

   c) What is typically the impact of Thumb mode and 32-bit ARM mode on performance
      in a system with:
      i) very slow memory
      ii) extremely fast memory
      Explain why!  
      (4 marks)

   d) How can ARM execute the following piece of C-code without using any branch
      command? Please explain how this can be done and give the assembly code for the
      C-code fragment! Assume that the values of the variables r1, . . . , r4 are already
      available in the registers with the same name.  
      (4 marks)

      ```
      if (r1 > r2) then
          r3 = r1;
          r4++;
      else
          r3 = r2;
          r4--;
      end if;
      ```

   e) The performance of the ARM7 core is heavily affected by the von Neumann bottleneck.
      What does this mean and give a solution to this problem (e.g. as used in ARM9)?  
      (2 marks)

   f) Considering the 3-stage pipeline of an ARM7 processor, give an example for an
      instruction that occupies the execute stage for
      i) one clock cycle,
      ii) an example for an instruction occupying the execute stage for two cycles, and
      iii) an example for occupying the execute stage for more than two cycles.  
      (3 marks)

   g) Why is required to restore the status register and the PC in one atomic step for
      returning from a SWI (also called SVC) system call?  
      (2 marks)
2. Questions concerning programming the ARM architecture

a) When do you use the branch command (B) and when the branch with link command (BL)? (2 marks)

b) Write ARM assembly code to perform the following array initialisation function (Assume that each integer is four bytes): (5 marks)

```assembly
function set_x42(int[] a, int elements)
    for(i=0; i<elements; i++)
        a[i] = x42
```

Additionally, assume that `a` is stored in memory and that the corresponding start address is in R0. Respectively, `elements` is stored in memory referenced by R1. Note that you don’t have to save any registers you might overwrite.

c) Describe the steps that have to be carried out by a (simple) operating system running on an ARM core to swap between two tasks (running in user mode). The swapping shall be triggered by a timer interrupt event. (8 marks)

d) The SWI (called SVC on later architectures) allows to pass an immediate value to the SWI (or SVC) handler. For example, `SVC # &42` is encoded as EF 00 00 42. How do you load an 8-bit value that is passed with an SWI or SVC command into register R0? (2 marks)

e) Write a program in ARM assembly language that computes the (even) parity of the content of register R0. Note that this is identical to a bitwise XOR over all 32 bits. The result shall be stored in register R1 (for example at bit position 0). (3 marks)
3. Questions about memory, memory management, and cache

a) Why is it necessary/useful to have several levels of memory in a system? Give an example for a system with at least four levels of memories! (4 marks)

b) What can be changed in the cache organization to save power consumption? Explain briefly why this saves power. (2 marks)

c) What can be changed in the cache organization to increase the hit rate without making the cache memory size larger? How does this impact implementation cost? (2 marks)

d) This question is related to paged memory management as it is used in ARM.
   i) Sketch the organisation of a simple 1-level paged memory system with 32-bit address space and 4Kbytes page size and describe the principles of its operation. (4 marks)
   ii) How big is the page table (in terms of bits)? (1 mark)

e) Describe briefly how a hard disk can be used to provide more memory than what is physically available as RAM and how the physical RAM is used? (3 marks)

f) Sketch the basic organisation of a Protection Unit for 8 memory regions as used in ARM and describe the principles of its operation? (4 marks)