Appendices: Figure 2 and Figure 3 – both sheets to be handed in with Answer books

COMP20241

Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

VLSI System Design

Monday 21st January 2008

Time: 09:45 - 11:45

Please answer any THREE Questions from the FOUR questions provided

This is a CLOSED book examination

The use of electronic calculators is NOT permitted.
Some questions refer to the 16-bit RISC processor, named STUMP, that you have been designing in the laboratory. Its Register Transfer Level (RTL) design for the datapath is given in Figure 1.

![Figure 1: RTL Design of 16-bit RISC Processor Datapath](image-url)
1. a) With the aid of a diagram, outline the stages of a design hierarchy and say why the use of such a hierarchy is essential in VLSI design. (4 marks)

b) Explain why three clock periods are used in the non-pipelined STUMP design to perform instructions; and explain why, although the pipelined STUMP design also uses three clock periods to perform an instruction, it has better performance. (3 marks)

c) Figure 2 (see Appendix at the back of the exam) shows an architectural view of the STUMP processor. By shading the path usage for each timing phase on Figure 2, show the usage of the non-pipelined STUMP when executing the *store* and *or* instructions in the code sequence below:

```
add r5, r0, #15  (add)
sub r4, r4, #1    (subtract)
st  r2, [r5, #0]  (store)
or r6, r6, r5    (or)
add r3, r3, #1    (add)
subs r0, r4, r1   (subtract)
```

(6 marks)

d) Using the same code sequence given in part (c), use Figure 3 to show the path usage when executing the *store* and *or* instructions in a 3-stage pipelined STUMP. (5 marks)

e) What useful checks do such path usage diagrams perform? (2 marks)

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2. a) What is meant by observability and controllability in the context of testable chip design? (2 marks)

b) Explain, using appropriate diagrams, the scan path approach to testability and describe how it operates. (8 marks)

c) What are the advantages and disadvantages of the scan path approach? (5 marks)

d) If the STUMP processor incorporated a scan path, discuss how this would make the testing of the processor easier. (5 marks)
3. a) What is meant by clock skew and explain how it arises. How might it affect a system? (5 marks)

b) In a chip, describe the measures that can be taken to minimise this skew. Illustrate your answer with a diagram of an iterated H clock-tree. (6 marks)

c) On your H clock-tree diagram from part (b), indicate the position of the clock generation logic, and discuss where the clock buffers should be placed in order to minimise the skew. (4 marks)

d) Discuss why clock skew is unlikely to be a problem in the STUMP design. (5 marks)

4. a) Control is usually implemented by:

   i) synthesis
   ii) ad hoc design
   iii) programmable logic array.

   Describe each of these approaches, giving the advantages and disadvantages of each. (8 marks)

b) In VHDL, models of hardware can be written at the behavioural, dataflow (or boolean) and structural levels. Explain what is meant by designs at these levels and state which would be the most appropriate for each design approach in part (a). (3 marks)

c) In the STUMP, the logic to implement the active-low memory read control signal is shown in Figure 4.

   ![Figure 4](image)

   Show in VHDL or pseudo code, how the hardware functionality of this logic would be described at the behavioural, dataflow and structural levels. (9 marks)

END OF EXAMINATION

Figures 2 and 3 follow on the next 2 pages
Non pipelined

Appendix

Figure 2

Don’t forget to hand BOTH your Figure 2 and Figure 3 sheets in with your Answer books

ID Number

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