Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

VLSI System Design

Wednesday 21st January 2009

Time: 14:00 – 16:00

Please answer any THREE Questions from the FOUR questions provided

The use of electronic calculators is NOT permitted.
Some questions refer to the 16-bit RISC processor, named STUMP, that you have been designing in the laboratory. Its Register Transfer Level (RTL) design for the datapath is given in Figure 1.
1. a) Explain, with the aid of a diagram, what is meant by a load/store architecture. (4 marks)

b) What are the three types of instruction that a load/store architecture can perform? (3 marks)

c) With reference to the diagram of the STUMP processor, explain how each of these instruction types is performed. (6 marks)

d) The STUMP processor has a 16-bit word. Discuss the hardware limitations this places on its design in terms of its load/store architecture. (3 marks)

e) In the STUMP, register R0 is permanently set to zero. Discuss the advantages and disadvantages of this and the impact on assembler code written. (4 marks)

2. a) In the Verilog hardware description language, what is meant by a blocking and non-blocking assignment? (4 marks)

b) What indicates a blocking and a non-blocking assignment? (2 marks)

c) Explain how blocking and non-blocking events are scheduled in the simulator. (6 marks)

d) Hence explain the values assigned to a and b in the code sequence given in:

   i) Figure 2a
   ii) Figure 2b

   **Figure 2a**  **Figure 2b**

   a = 1;  a = 1;  
   b = 2;  b = 2;  
   a = b;  a ← b;  
   b = a;  b ← a;  

   (6 marks)

e) If the Verilog description is ambiguous in describing the desired logic, what is the likely outcome in simulation and in synthesis? (2 marks)
3. 
   a) What is meant by observability and controllability in the context of testable chip design? (3 marks)
   b) With the aid of a diagram, describe the operation of signature analysis in detecting errors in chip designs. (6 marks)
   c) Discuss the advantages and disadvantages of the signature analysis approach to error detection. (5 marks)
   d) How might you establish the required signature for a chip? (3 marks)
   e) If you were incorporating signature analysis logic into the STUMP, which point(s) would you select as your input data to this test logic and why? (3 marks)

4. 
   a) Discuss the essential differences between datapath logic and the logic for control. (3 marks)
   b) Hence explain what is meant by a “bit slice approach” for datapath logic. (3 marks)
   c) What are the advantages of a “bit slice approach” and what information does it convey to the designer? (4 marks)
   d) If synthesising a datapath, would you expect the resulting design to be more or less efficient than doing a “bit slice design”. Explain. (3 marks)
   e) Briefly outline the steps that need to be taken in semi-custom design after the logic design stage in order to submit the design for manufacture. (7 marks)