请回答问题 ONE 和一个问题来自问题 TWO 或 THREE 中的一个。

电子计算器的使用是允许的，前提是它们不具有编程功能且不存储文本。
1. **COMPULSORY**

Answer any **ten** subsections of this question. Each part is worth 2 marks.

a) Sketch a schematic for a 2 input XNOR gate constructed from AND, OR and NOT gates.

b) Describe a 4:1 multiplexer using Verilog.

c) The diagram below shows the behaviour of a counter. Continue the diagram showing what happens if
   i) the reset is synchronous
   ii) the reset is asynchronous.

![Counter Diagram]

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d) Give two examples of CAD tools which are used in digital hardware design and briefly state what each is used for. [Brand names of tools are not required.]

e) What component is represented by the following Verilog?

   ```verilog
   reg [31:0] q;
   always @ (en, d)
       if (en) q = d;
   ```

f) Briefly explain why a D-type flip-flop is a good basic model for designing synchronous FSMs.

g) What are the main differences between static and dynamic RAM and which would be better for implementing a fast cache?

h) Explain why tri-state devices might be required for connection to a processor data bus.

i) Explain what type of preconditioning must take place to allow two eight bit binary values to be subtracted using an eight bit adder.

(Question 1 continues on the following page)
(Question 1 continues from the previous page)

j) What is the main function of the program counter register and why is it necessary to do more than just increment and decrement this register by one?

k) Give two reasons for the desirability of designing complete systems on a single silicon chip.

l) In a display system there are 1024 by 512 pixels and each pixel has 256 possible grey levels. If this display is mapped to 8 bit wide memory, how many address lines will be required to address the whole display space?

2. a) What are the advantages and disadvantages of serial compared to parallel communication in a computer system? Giving your reasons, state which type of communication would be better in the following cases:

i) A high bandwidth data bus on a processor chip.
ii) A printer positioned some distance from the computer.
iii) A multifunction keyboard attached to a desktop PC.  

b) Serial data can be transmitted in a synchronous or asynchronous fashion. Explain the main differences between these two types of serial data transmission and how using separate wires for clock and data signals can be avoided.

c) An asynchronous serial data transmission consists of eight data bits, one start bit, one stop bit and one parity bit. Explain the purpose of the start bit, stop bit and parity bit.

d) In the example given in Q2(c) one bit is transmitted in 100 microseconds. The serial link is set up to transmit over a 10 kilometre long wireless link. Calculate the bandwidth of the channel in bytes per second for data transmission and its approximate latency from transmitter to receiver given the speed of light is $3 \times 10^8$ m/s.
The following is an almost complete Verilog module specification.

```verilog
module mystery (input wire clk,
    input wire reset,
    input wire start,
    input wire [9:0]a,
    input wire [9:0]b,
    output wire busy,
    output reg [19:0]c);

reg state;
reg [9:0]x;
reg [9:0]y;

always @(posedge reset, posedge clk)
    if (reset) state <= 0; //Reset
    else
        case (state)
            0: if (start) //Initial state
                begin
                    state <= 1;
                    c <= 0;
                    x <= a;
                    y <= b;
                end
            1: if (x == 0) //Iterate until x == 0
                begin
                    if (!start) state <= 0;
                    end
                else
                    begin
                        if (x[0] == 1) c <= c + y; // AA
                        x <= x >>1; // shift right
                        y <= y + y; // BB
                    end
        endcase
endmodule
```

a) Explain, in words, what the test in line AA is doing. (2 marks)

b) How might line BB be constructed without needing an adder? (2 marks)

c) Sketch and label a state diagram of this machine. (2 marks)

d) Choose some input data values for “a” and “b”. Show, using a table, a timing diagram or other means of your choice how the system will process these inputs following “start” becoming active. [Recommendation: choose values between 10 and 20.] (6 marks)
(Question 3 continues from the previous page)

e) What function of “a” and “b” is present on “c” when the process is complete? (2 marks)
f) Briefly state what is meant by a “handshake” between state machines. (3 marks)
g) The wire “busy” is not defined above. What needs adding to the code to allow this to handshake with “start”? (3 marks)