One and a half hours

Question 1 compulsory

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Fundamentals of Computer Engineering

Date: Monday 24th January 2011
Time: 09:45 - 11:15

Please answer Question ONE and one other Question from either Questions TWO or THREE

This is a CLOSED book examination

The use of electronic calculators is permitted provided
they are not programmable and do not store text

[PTO]
1. **COMPELLSORY**

Answer any ten subsections of this question. Each part is worth 2 marks.

a) State DeMorgan’s theorem and use it to derive an alternative expression for the XOR function:

\[ F = \overline{A}B + A\overline{B} \]

that permits its implementation using NAND gates only.

b) Produce the truth table and sketch a schematic diagram for a 2:1 multiplexer.

c) Sketch a simple datapath structure for a clocked RTL (Register Transfer Logic) system, and briefly discuss the important aspects of the system.

d) The following Verilog statement is used to describe a component in a module

```verilog
always @ (clk, d)
  if (clk) q=d;
```

and the following stimulus file is used to check its behaviour

```verilog
initial clk = 0;

always begin
  #50
  clk = ~clk;
end

initial begin
d = 0;
  #25
d = 1;
  #50
d = 0;
  #50
d = 1;
$stop;
end
```

Produce a timing diagram illustrating the waveforms for all signals after running the simulation.
e) Represent the following decimal values using 4-bits in two’s complement form where possible. If not possible, please explain why:

i) 0
ii) 7
iii) -7
iv) 12

f) What is the difference between blocking and non-blocking assignments in Verilog? Is it possible to mix blocking and non-blocking assignments in the same statement?

g) Explain what Direct Memory Access (DMA) means and give an example of where DMA would be useful.

h) Give two properties of program code that allow the use of fast memory caches to improve performance.

i) Given that a microprocessor has an 8 bit data bus and a 16 bit address bus, how many 8 bit memory locations can it address?

j) Give the sequence of events taking place in a parallel data exchange using a two wire handshake.

k) What is a “hardware interrupt” and give an example of its use?

l) What does saying that a bus is “multi-master” mean. Giving your reasons state which of the following cannot be used as a multi-master bus:

i) I²C bus.
ii) Processor bus with a non tri-state address bus.
2. a) Giving your reasons indicate which of the following statements is true and which is false:

i) Bandwidth can be measured in seconds. \hspace{1cm} \text{(1 mark)}

ii) The bandwidth of cache memory is higher than the main memory bandwidth. \hspace{1cm} \text{(1 mark)}

iii) Increasing bandwidth always decreases latency. \hspace{1cm} \text{(1 mark)}

iv) Adding latches to a pipeline increases latency. \hspace{1cm} \text{(1 mark)}

b) Explain how the use of a pipeline can increase both bandwidth and latency, illustrating your answer with the example of a three-stage instruction pipeline. \hspace{1cm} \text{(6 marks)}

c) Why does the above pipeline not give a three times increase in speed in practice, and what must be done to optimise the pipeline design? \hspace{1cm} \text{(6 marks)}

d) A processor has a three stage instruction pipeline. Indicate the state of this pipeline when the JMP instruction in the following code sequence is executed.

```
ADD Sum;
STO Sum;
JMP wombat;
LDA Test;
SUB Sum;
```

Hence determine the minimum latency in clock cycles of such a pipeline? \hspace{1cm} \text{(4 marks)}
3. a) Using the symbol for a D-type transparent latch, sketch a possible implementation of a D-type flip-flop and explain its behaviour. You may use additional NOT gates as required.  

b) Produce a sketch of the basic structure of a finite state machine, labelling its significant components. Briefly explain the purpose of these components.  

c) A “stopwatch” counter exhibits the following behaviour:  

The counter displays a 3-bit count and when started counts from 000 to 111 and then stops.  

The counter increments at a rate determined by the frequency of the applied clock signal.  

The stopwatch has three input signals to control its behaviour:  

**start**: Initially the counter is in state zero and only starts counting when the start signal goes high. Once counting the start signal has no effect.  
**stop**: If the counter is counting and the stop signal is high, then the counter remains at the current count, otherwise it has no effect.  
**reset**: If the reset signal is high, then the counter returns to the initial state of zero where it remains until the start signal is asserted again.  

The start, stop and reset signal are mutually exclusive, i.e. they cannot be applied at the same time.  

Produce a state transition diagram to illustrate the described behaviour of the required counter.  

d) Translate your state diagram into a Verilog description that can be synthesized into hardware.  

e) Give two Verilog statements that are not typically synthesizable, in each case say why.