Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

VLSI System Design

Date: Tuesday 25th January 2011
Time: 09:45 - 11:45

Please answer any THREE questions from the FOUR questions provided

This is a CLOSED book examination
The use of electronic calculators is NOT permitted
Some questions refer to the 16-bit RISC processor, named STUMP, that you have been designing in the laboratory. Its Register Transfer Level (RTL) design for the datapath is given in Figure 1.
1. a) With the aid of a diagram, briefly describe the stages of a design hierarchy down to the logic level for silicon chip design and state why such a hierarchy is adopted. (6 marks)

b) The Top Level Model is an external view of the chip. Discuss why this Model is an essential stage in the design process. (3 marks)

c) In the Top Level Model for the STUMP processor, the least significant 8 or 5 bits of the Instruction Register (I[15:0]) are sign extended to 16 bits depending on whether the instruction is a branch (I[15:13]) or not. Write a Verilog task which can be called to perform this action. (8 marks)

d) If the Top Level Model were to describe the behaviour of a pipelined STUMP, would this behaviour be different from a non-pipelined STUMP? If so, how would this arise? (3 marks)

2. a) Four functional blocks can be identified in the architecture of the STUMP processor. State what these are and explain the purpose of each block. (6 marks)

b) Ten components are shown in the RTL diagram of the STUMP processor in Figure 1. For each component, state which functional block at the architectural level the component belongs to. (5 marks)

c) By identifying the register(s) on Figure 1 used for holding the output of each pipeline stage in a pipelined STUMP, discuss why the datapath for a pipelined and non-pipelined STUMP is identical. (5 marks)

d) With the aid of a timing diagram, explain why an additional register in Control is needed if converting from a non-pipelined to a pipelined STUMP design. (4 marks)
3. a) What is meant by synchronous design? Why is it a generally preferred approach rather than asynchronous timing? (5 marks)
b) Explain what is meant by the “basic gate delay $\tau$” when referring to the propagation delay through digital logic. (3 marks)
c) Describe how a knowledge of $\tau$ can be used to predict the delay through a chain of gates whose size increases by a factor $n$ at each stage. Illustrate your answer with reference to a factor $n$ of 4 used to eventually drive a load of 256. (7 marks)
d) Describe how scaling down transistor sizes and voltages affects the gate propagation and interconnection delays. What effect is this likely to have on the chip timing? (5 marks)

4. a) What is meant by controllability and observability in the context of testable chip design? (3 marks)
b) Describe, with the aid of a diagram, the test bench used to test the STUMP processor. (6 marks)
c) Describe, with the aid of a diagram, the scan path approach to testing. (6 marks)
d) Compare the features of a STUMP incorporating a scan path with the test bench approach adopted in the laboratory for testing the STUMP processor. (5 marks)

END OF EXAMINATION