One and a half hours

Question 1 compulsory

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Fundamentals of Computer Engineering

Date: Monday 23rd January 2012
Time: 14:00 - 15:30

Please answer Question ONE and one other Question from either Questions TWO or THREE

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text
1. **COMPULSORY**

Answer any ten subsections of this question. Each part is worth 2 marks.

a) What is a register used for? Sketch a schematic of a 4-bit register with clock and enable control inputs.

b) Describe how the use of abstraction in digital design can help simplify the design process.

c) State the decimal values for the following 5-bit binary numbers that are using 2’s complement representation.

   i. 00000
   ii. 01111
   iii. 10101
   iv. 11111

d) Complete the following Verilog module to describe a 4:1 multiplexer.

   module mux_4_1 (d, s, q);
   input [3:0] d;
   input [1:0] s;
   output q;

   < Your code here>

   endmodule

e) The logical expression for a 2-input XNOR gate with inputs A and B is

   \[ Q = \overline{A} \overline{B} + A \overline{B} \, . \]

   Sketch a schematic for the XNOR gate constructed from AND, OR and NOT gates only.

f) Describe the terms setup time and hold time in relation to the design of sequential systems. Why must care be taken to ensure that the input data does not change during these times?

g) What assumptions must be made if a process pipelined into N stages is to go N times faster than the equivalent non-pipelined system?
h) In memory data transfer explain what is meant by a wait state and why it might be required?

i) Explain why it might be necessary to use a tri-state output device on an address bus.

j) Explain the need for start and stop bits in RS232 serial data transmission and indicate how a parity bit can be used to check data integrity.

k) Give two reasons for the desirability of designing complete systems on a single silicon chip.

l) Place the following memory types in order from fastest data access to the slowest and explain what each memory type might be used for in a practical system.

   i. Flash memory
   ii. Dynamic RAM
   iii. SRAM
   iv. Battery backed CMOS RAM
2. a) The following code is a Verilog description for a simple state machine controller.

    module controller (clock, digit);
    input   clock;
    output  [3:0] digit;
    reg     [3:0] digit;
    reg     [3:0] next_state;
    reg     [3:0] current_state;
    always @ (current_state)
      if (enable == 1)
        case (current_state)
          0: next_state = 1;
          1: next_state = 2;
          2: next_state = 3;
          3: next_state = 4;
          4: next_state = 5;
          5: next_state = 6;
          6: next_state = 7;
          7: next_state = 8;
          8: next_state = 9;
          9: next_state = 0;
          default: next_state = 0;
        endcase
    endmodule

i. Describe the general structure of a Verilog module. 
(2 marks)

ii. What does the declaration on the line indicated by “1:” do? 
(1 mark)

iii. When will the always block on the line indicated by “2:” be executed? 
(1 mark)

iv. What is the difference between the assignments = and <=? 
(2 marks)

(Question 2 continues on the following page)
A modulo-7 counter is required to count on the rising edge of an input signal clock. If an external signal stop is high then the counter is required to stop at the current count, and should only continue to count when the stop signal goes low. In addition, the counter requires two output signals, odd and even, that are used externally to control a display to indicate whether the current count is odd or even (0 can be treated as even).

Produce a state transition diagram to describe the behaviour of the required counter.

(4 marks)

c) Select state codes for each state in your state transition diagram for part b) and draw a state transition table for your design.

(5 marks)

d) Produce a Verilog description of a module to describe the behaviour of your counter design.

(5 marks)
3. a) Figure Q3 shows the datapath of a simple processor (MU0). Explain the function of the three registers (ACC, PC and IR) in the system. How general are these registers in processor systems?

   (4 marks)

b) How many states are required in the timing and control state machine to operate this simple processor and suggest a simple implementation to control the state transition?

   (3 marks)

c) Describe what information is present on each of the five labelled busses (Data-Out, Address, Data-In, PC-OUT, ALU-OUT) during an instruction fetch operation.

   (5 marks)

Figure Q3

(Question 3 continues on the following page)
(Question 3 continues from the previous page)

d) The ALU consists of a 16-bit adder and two input pre-conditioners for the X and Y bus inputs. What is the purpose of the preconditioners? List the function of the two pre-conditioners during an instruction fetch and the execution of SUB and JUMP instructions.

(5 marks)

e) What modifications would need to be made to allow the JUMP instruction to take one clock cycle instead of two?

(3 marks)