Fundamentals of Computer Engineering

Date:      Tuesday 22nd January 2013
Time:     14:00 - 15:30

Please answer Question ONE and ONE other Question from either Questions TWO or THREE

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text
1. **COMPULSORY**

Answer any ten subsections of this question. Each part is worth 2 marks.

a) What is hierarchy with respect to digital design? Give an example of the use of hierarchy in a design.

b) Identify the four possible states of a single bit binary signal.

c) Using De Morgan’s theorem derive an alternative expression for the function:

\[ Q = X \cdot Y + \overline{X} \cdot \overline{Y} \]

that can be implemented using only OR and NAND gates. Sketch the circuit. You may assume that inverted signals \( \overline{X} \) and \( \overline{Y} \) are provided for you.

d) Provide a sketch of a register transfer level (RTL) datapath. Discuss its key components.

e) Discuss when variables of type `wire` and `reg` should be used in Verilog assignments.

f) A simple flip-flop can be described using the following Verilog module.

```verilog
module flip_flop(D, clk, Q, Qbar);
  input D, clk;
  output Q, Qbar;
  reg Q, Qbar;
  always @(posedge clk)
  begin
    Q <= D;
    Qbar <= ~D;
  end

endmodule
```

Produce a modified module description that incorporates an enable signal input, `En`, that only allows the outputs to be reassigned when `En = 1`.

(Question 1 continues on the following page)
(Question 1 continues from the previous page)

**g)** What is the function of the *program counter register* and what is the value in the programme counter immediately after execution of the jump instruction in the following MU0 code fragment?

```
0C00:  LDA data;
0C01:  SUB diff;
0C02:  JGE 0C15;
0C03:  ..... 
```

Data    DEFW 25;
Diff    DEFW 26;

**h)** What is meant by *non-volatile memory* and why is it necessary in a computer system?

**i)** Given that a microprocessor has a 16-bit data bus and a 16-bit address bus, how many 16-bit memory locations can it address? Most current processors use 8-bit byte addressing, how could this be accomplished?

**j)** What preconditioning is required to allow a 16-bit full adder to do a 16-bit subtraction?

**k)** What is meant by a *hardware interrupt* and give two examples of where such interrupts might be required?

**l)** Give two reasons for the desirability of designing complete systems on a single silicon chip.
2. a) A student was required to design a finite state machine for a lab project. The first stage in the design process was to produce a state transition diagram to illustrate the transition between states, and the influence of the input signals on the state transitions. Figure Q2.1 illustrates a sketch of the student’s state transition diagram, which unfortunately contains a number of errors. Identify the errors in the state transition diagram.

(3 marks)

b) You are required to design a finite state machine (FSM) to control a vending machine that will dispense a chocolate bar costing 30 pence when the correct money is entered. The vending machine accepts only 10 pence coins and should wait until three 10 pence coins are entered before the chocolate bar is dispensed. The required FSM has the following input and output:

Input:
coin_10p – goes high when a 10 pence coin has been entered, it is 0 otherwise.

Output:
dispense – should go high once three 10 pence coins have been entered, it should be 0 otherwise.

(Question 2 continues on the following page)
From the specification we can identify that the design will require 4 states, as illustrated in the incomplete state transition diagram in Figure Q2.2.

Sketch a completed state transition diagram for the required FSM that illustrates ALL state transitions, the condition of the input, coin_10p, that determines these transitions, and indicates the state where the output, dispense, is asserted.

(4 marks)

![Figure Q2.2](image)

**Figure Q2.2**

c) Assign state codes to each state in your completed state transition diagram from part b) and produce a state transition table.

(5 marks)

d) The manufacturer has changed the specification for the vending machine and decided that the machine should also accept 20 pence coins in addition to 10 pence coins. Consequently, an updated FSM design must be produced in order to provide the extra functionality required for payment with 10 pence and 20 pence coins. The cost of the chocolate bar remains unchanged at 30 pence. However, the machine should dispense a chocolate bar whenever the correct combination of 10 pence and 20 pence coins has been entered. An additional input signal, coin_20p, is provided that goes high if a 20p coin has been entered. If two 20 pence coins have been entered then a new output “change” should be asserted, which will release 10 pence in change. Produce a modified state transition diagram for the new controller, introducing new states where required. Please note: the inputs coin_10p and coin_20p cannot both be high at the same time.

(8 marks)

[PTO]
3. a) Using a simple diagram explain what is meant by the “Three Box Model” of a computer system. Describe the function of the three main busses that connect the boxes in the model.

   (6 marks)

b) Why is it necessary to provide peripheral interfaces rather than connect input/output devices directly to the busses?

   (2 marks)

c) A peripheral interface is used to provide an 8-bit data port to connect to a printer with an 8-bit parallel input. The peripheral interface has three registers:

   a. A data register to hold input/output data
   b. A data direction register to control which bits are input and which output
   c. A control/status register to set the operating mode of the port and read the state of any control lines.

   The 8-bit printer connected to the port uses a simple two wire handshake protocol using two control signals DAV (data available) and ACK (data acknowledge) provided by the peripheral interface. Describe the sequence of events that will take place when a byte of data is output from the port to the printer using this simple protocol.

   (4 marks)

d) Draw a simple schematic diagram to show how changing the value of a bit in the direction register could set the data direction of the corresponding bit in the data port.

   (6 marks)

e) What are the consequences for the DAV and ACK lines of changing the port data direction from output to input?

   (2 marks)