Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Processor Microarchitecture

Date: Thursday 22nd January 2015
Time: 14:00 - 16:00

Please answer any THREE Questions from the FOUR Questions provided

Use a SEPARATE answerbook for EACH Question.

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text
1. a) Identify two characteristics of a RISC processor that distinguish it from other designs (such as RISC).  
   (2 marks)

b) The Stump processor uses five different addressing modes: immediate, register, offset, PC relative and indexed. Briefly describe two of these addressing modes, using diagrams where appropriate, and state for each case a Stump instruction that uses the addressing mode discussed.  
   (4 marks)

c) The Stump processor is a RISC processor with eight programmer registers. Outline briefly the special function of two of these registers.  
   (2 marks)

d) Stump has a status register containing four flag bits: N, Z, V, and C. Discuss the operation of each flag. If you only have access to the two operands, the result, and the operation (ADD, SUB, etc.) how could you determine whether the N, Z, and V flags should be set?  
   (4 marks)

e) Figure 1 gives a short code sequence for the Stump processor. Identify for each instruction executed the register or memory address that is updated, and the new value(s) after the instruction has been executed.  
   (8 marks)

; The following registers are predefined
; (values in hex unless specified otherwise):

; R0 = 0x0000
; R1 = 0xD010
; R2 = 0x0FA5
; R3 = 0x2F6A
; R4 = 0xFFFF
; R5 = 0xD011
; R6 = 0x000B
; R7 = 0x0101
; CC = 0b0001

ORG 0x101
ADD R0, R1, #0x4
ADCS R5, R3, R5
BCS L0
OR R1, R1, #0x1
SUBS R4, R5, R1
BEQ L1
L0: ST R4, [R6, #0x4]
L1: ST R1, [R2, #0xF]

ORG 0xF
DATA 1234

ORG 0xFB4
DATA AB41

Figure 1
2. a) Figure 2 illustrates the register transfer level (RTL) design of the datapath in Stump. Explain using the key features in this diagram how the Stump processor performs the following operations: (4 marks)

i. a Type 1 instruction,
ii. a Type 2 instruction,
iii. a Type 3 instruction,
iv. load/store instructions.

![Diagram of Stump processor's datapath](image)

**Figure 2**

(Question 2 continues on the following page)
(Question 2 continues from the previous page)

b) The RTL datapath in Figure 2 illustrates a sign extender and a shifter. Briefly discuss the operation of these two functional blocks. (2 marks)

c) Produce Verilog modules to describe the behaviour of the Stump shifter and Stump sign extender. The required input and output signals to each block are illustrated in Figure 2. In the case of the shifter block, the required operation is illustrated in Figure 3.

In the case of the sign extender the operation of the module can be determined directly from the instruction, where a branch instruction can be identified by bits [15:13] of the instruction being 111. (14 marks)
3. a) What is the chief feature which distinguishes a Harvard architecture from a von Neumann architecture? (2 marks)

b) Briefly describe one advantage of each of the above architectures over the other. (4 marks)

The AVR processor, as used in Arduino boards, is an '8-bit' processor with a Harvard architecture. Unlike an ARM, Stump etc. its 'registers' are not in a separate logical address space but act as aliases for the first 32 bytes of the 64K data memory.

c) How many bits are needed for a general data memory address? (2 marks)

Most AVR instructions - and all data processing instructions - are 16 bits long.

d) What advantage to the ISA design is conferred by having these ‘short’ register addresses rather than using a ‘full’ address each time? (2 marks)

e) Why is the destination ‘register’ always the same as one of the source registers in ADD, SUB etc. operations? (2 marks)

A typical use of an AVR is as a single-chip controller programmed with a fixed function.

f) Sketch a block diagram showing all of an AVR system’s storage spaces which are visible to the programmer (i.e. in the ISA). The implementation should be optimised for performance. For each part, clearly show the dimensions (where known) and storage technology employed. The sketch should show the bus connections but the processing components (ALU, multiplexers etc.) and the control logic may be abstracted as a ‘black box’. (8 marks)
4. a) For a given size of silicon die, estimate how many more components could be available when shrinking from a 28nm process to a 21nm process. (2 marks)

b) Instead of adding transistors, an existing logic circuit is shrunk onto the new process. Give three benefits that might be expected, briefly explaining the reason(s) in each case. (6 marks)

c) Why are standard cells typically used for the layout of logic on a silicon die, rather than using custom-drawn structures? (2 marks)

d) Why would standard cells typically not be used for the layout of memory (e.g. for code cache) on a silicon die? (2 marks)

e) After placing and routing a chip’s layout it is usual to ‘extract’ physical characteristics using the appropriate CAD tools. Which characteristics are of chief interest for the late stages of simulation? (3 marks)

f) One CAD tool which is used late in the layout process is ‘DRC’. What does this stand for and what does the tool do? (2 marks)

g) A technique which is now starting to be introduced is stacking chips in 3D. What effect might this have on the power dissipation of the system? Justify your answer. (3 marks)

END OF EXAMINATION