COMP 12111

One and a half hours

Section A is COMPULSORY

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Fundamentals of Computer Engineering

Date: Monday 23rd January 2017

Time: 09:45 - 11:15

Answer BOTH Questions in Section A and ONE Question from Section B

Use a SEPARATE answerbook for each SECTION.

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text

[PTO]

Section A

COMPULSORY

Please Answer BOTH Question 1 and Question 2

1. Answer any **5** parts of this question. Each part is worth 2 marks.

   a) What are the four possible states used for simulating a single bit binary signal? (2 marks)

   b) What is DeMorgan's theorem? State it and then use it to derive an alternative expression of the XOR function.

   $$F = \bar{C}.D + C.\bar{D}$$

   that enables its implementation using 3 NAND gates. Sketch a schematic of the NAND gate implementation. You may assume that inverted signals $\bar{C}$ and $\bar{D}$ are made available. (2 marks)

   c) When are blocking and non-blocking assignments used in Verilog? What symbols are used for each? What is the difference between blocking and non-blocking assignments in Verilog? Is it possible to mix blocking and non-blocking assignments in the same always block? (2 marks)

   d) What is abstraction with respect to digital design? What does it help with? Provide an example of the use of abstraction in a design. (2 marks)

   e) When should you use type *wire* and when type *reg* for variables in Verilog assignments? (2 marks)

   f) Sketch an equivalent schematic representation of the logical function described by the Verilog module given in Figure 1. (2 marks)

```
module acircuit (input  A, B, C,
                 output  Q);

wire avariable;

assign avariable = A&~B;
assign Q = C | avariable;

endmodule
```

Figure 1

g) What is a register used for? What is a register constructed from? Sketch a schematic of a typical 2-bit register with clock and clock-enable control inputs, clearly indicating the inputs and outputs. (2 marks)

h) Do signals change state instantaneously in digital circuits? Please define the terms set-up time, hold time and propagation delay with respect to synchronous circuits. Figure 2 depicts the behaviour of a D-type flip-flop where Clk is the clock input, D is the data input and Q is the output. Copy the waveforms shown in Figure 2 in to your answerbook and illustrate set-up time, hold time and propagation delay on your sketch. (2 marks)

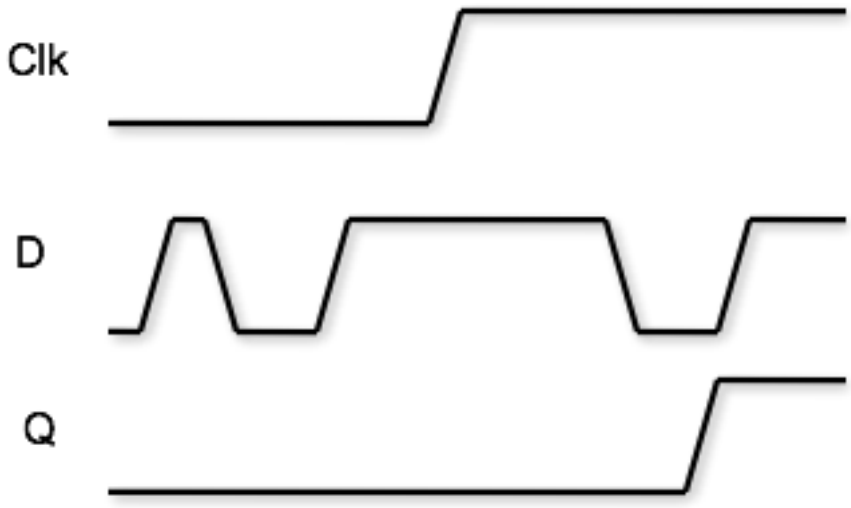

Figure 2

[PTO]

2. Answer any **5** parts of this question. Each part is worth 2 marks.

a) Discuss the difference between von Neumann and Harvard architectures. State one advantage and one disadvantage of the Harvard architecture compared to the von Neumann architecture. (2 marks)

b) What is meant by 'volatile memory'? Give an example. (2 marks)

c) Draw the symbol for the tri-state buffer. Briefly discuss its operation. (2 marks)

d) What is DMA and why is it used? (2 marks)

e) Figure 3 shows a simple combinatorial circuit to be used as part of an RTL design. For the technology used the gates with output inversion have a delay of 2ns, and the gates with no output inversion have a delay of 3ns. Determine the critical path of the circuit. What would be the maximum clock frequency that the RTL system can be operated at? (2 marks)

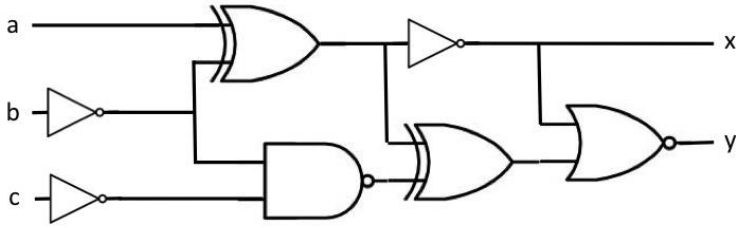

Figure 3

f) The design of an embedded processor has a 16-bit address bus and a 16-bit data bus. Due to cost limitations the maximum memory size allowed is 16K and the memory chips chosen are a single byte wide and can support 4,096 memory locations. How many of the 16 bits of the address bus are used to address the memory? How many memory chips will be required to implement the required memory? (2 marks)

g) The three box model of a computer consists of the processor, memory and input/output. It also has a system bus to connect these components together. Briefly explain what the system bus is. Why do we need an interface circuit between the system bus and the external peripheral? (2 marks)

h) You are part of he design team for the latest games console. You are required to arrive at the design for the head for the optical drive and must choose a laser and objectives lens to satisfy the specifications. Identify a choice for laser wavelength and objective lens numerical aperture from the list below to maximise the storage capacity of the disk. Explain your answer. (2 marks)

Laser Wavelength: 405nm, 532nm, 640nm
Objective lens numerical aperture: 0.6, 0.7, 0.85

Section B

Please answer ONE Question from Questions 3 and 4

3.

a) You are required to design a Finite State Machine (FSM) to capture the behaviour of a vending machine. The vending machine dispenses your favourite soft drink that cost 20 pence. The vending machine accepts only 10 pence coins and should wait until all the coins are entered before the soft drink is dispensed. The vending machine does not give change.

The required FSM has the following input and output:

Input: **coin_10p** – it goes high when a 10 pence coin has been entered; it is 0 otherwise.

Output: **dispense** – it should go high once two 10 pence coins have been entered; it should be 0 otherwise.

From this specification we can identify that the design will require 3 states, as illustrated in the incomplete state transition diagram in Figure 4.

Sketch a completed state transition diagram for this FSM that illustrates ALL the state transitions and the condition of the input, coin_10p, determining the transitions. Make sure you also indicate the state where the output, dispense, should be taken high. (6 marks)

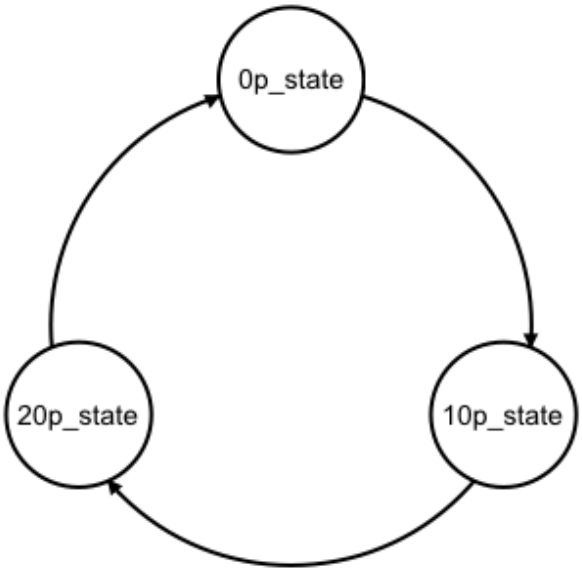

Figure 4

[PTO]

b) How many bits are required in the state code to be able to represent all the states in the FSM? (1 mark)

c) Assign unique state codes to each state in your completed state transition diagram from part a). (1 mark)

d) Produce a state transition table indicating the current state, the input, the next state and the output. (4 marks)

e) The price of the soft drink is increased to 30p and the vending machine altered to also accept 20 pence coins in addition to 10 pence coins. The vending machine should dispense a drink by taking the output **dispense** high whenever the correct amount has been entered. If too much has been entered then the vending machine should dispense the drink and give change by taking an additional new output, **change**, high. An additional new input is provided, **coin_20p**, that goes high when a 20 pence coin has been entered; it is 0 otherwise.

Due to the design change the FSM needs changing to capture the additional functionality reflecting the higher cost, that 20p and 10p coins are now accepted for payment, and that change is given.

Produce a new state transition diagram for the FSM of the updated vending machine, introducing new states where required. Please note: the inputs coin_10p and coin_20p are mutually exclusive. (8 marks)

4. a) In the design of a processor what is the purpose of the control block? (2 marks)

b) Discuss which status flags are provided in the design of MU0. Where are they used in the general operation of MU0? Give examples where appropriate. (3 marks)

c) Figure 5 shows a design for the datapath of MU0.

i) Discuss the function of these registers Acc, PC and IR. (3 marks)

ii) What are the four operations provided by the MU0 ALU. (2 marks)

d) In the datapath shown in Figure 5 seven buses in the MU0 datapath are highlighted and labelled. Discuss what information is present on each of these buses for the following:

i) during an instruction fetch (3 mark)
ii) during the execute state of an LDA instruction (4 mark)
iii) during the execute state of a branch instruction. (3 mark)

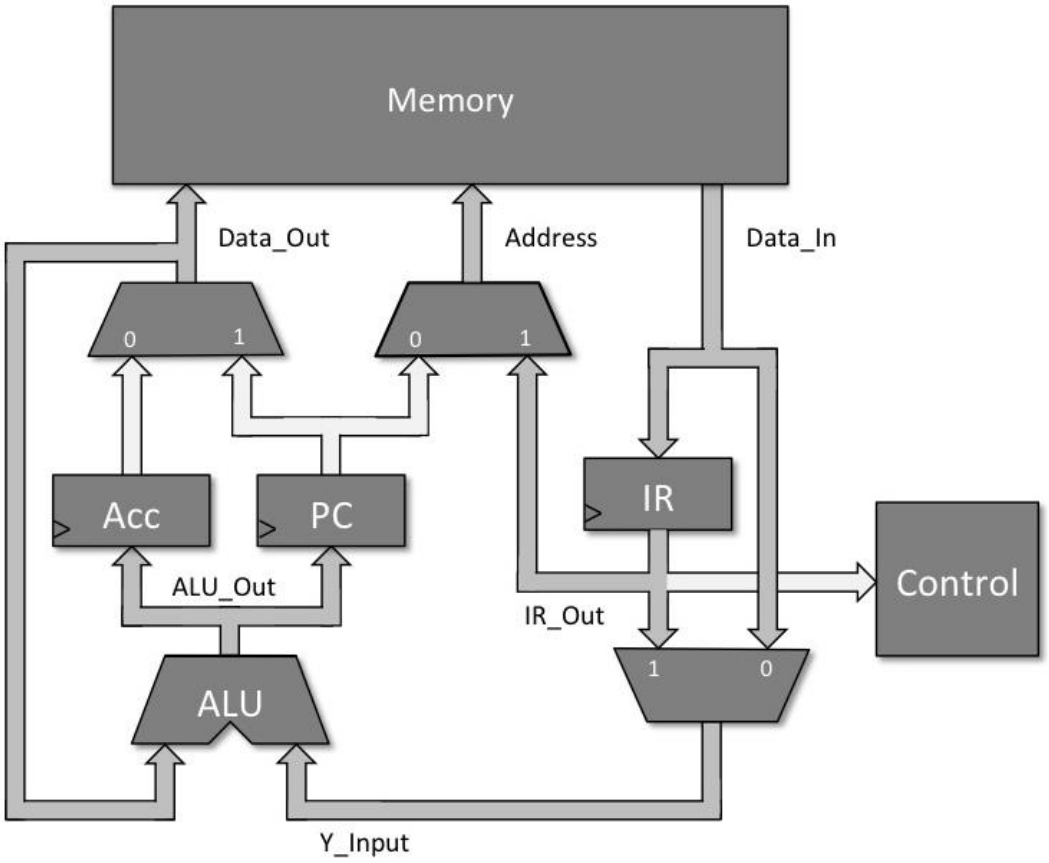

Figure 5

END OF EXAMINATION