COMP 12111

Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Fundamentals of Computer Engineering

Date: Friday 26th January 2018

Time: 14:00 - 16:00

Please answer all FOUR Questions.

Use a SEPARATE answerbook for each QUESTION.

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text

[PTO]

1.

a) What is **hierarchy** with respect to digital design? Provide a design example of the use of hierarchy.

What is **abstraction** with respect to digital design? How does abstraction assist the designer? (2 marks)

b) How many states can be represented using 1 byte (8-bits)? What are the equivalent one byte (8-bit) 2's complement binary representations of the following signed decimal values? (2 marks)

i) -2
ii) -129
iii) 127

c) For what input conditions will the 2-input NAND logic gate produce a true output? Produce a Boolean expression for the NAND function. Why is the NAND gate often referred to as a **universal logic gate**? (2 marks)

d) Sketch an equivalent schematic representation of the logical function described by Verilog module given in Figure 1. Which equivalent popular logic gate is being implemented? (2 marks)

```
module afuncircuit ( input    a, b,
                     output   q);

wire  avariable;
wire  bvariable;

  assign   avariable = ~a & b;
  assign   bvariable = ~a | b;
  assign   q = ~bvariable | avariable;

endmodule
```

Figure 1

e) State DeMorgan's theorem as Boolean expressions. Using DeMorgan's theorem derive an alternative expression for the simple logic function:

$$Q = \overline{((A + \overline{B}).(\overline{A} + B))}$$

Which logic function does this represent? (2 marks)

2.

a) Why is Non-Return-To-Zero Inverted (NRZI) encoding used for the transmission of data via USB? Sketch the transmitted waveform for the following data when encoded using NRZI. (2 marks)

… 1 0 1 0 1 1 1 1 0 0 1 …

b) In a particular computer system, the critical path delay is related to the maximum delay through the ALU, which is 25ns. You have clock speeds of 10MHz, 20MHz, 50MHz and 100MHz to choose from. Which clock speed would you select to give you optimum performance and why? (2 marks)

c) What is meant by non-volatile memory? Give an example. Why is some non-volatile memory essential in a computer system? (2 marks)

d) What technique is used for transferring large blocks of data to/from main memory? Provide a brief description of its operation. (2 marks)

e) Explain the role of the *program counter* (*PC*). A design for a RISC processor has an 8-bit address bus and a 16-bit data bus, if the memory used only has 8-bit memory locations, by how much should the *PC* be updated every fetch cycle?

(2 marks)

[PTO]

3.

a) What is a **multiplexer**? How many select lines does an 8:1 multiplexer require?

(1 mark)

b) Draw the symbol for the 4:1 multiplexer, clearly labelling the inputs and outputs. (2 marks)

c) Produce a Verilog module called "multiplexer" that provides the functionality of the 4:1 multiplexer. You may use continuous assignment or blocking assignment in your module design. (5 marks)

d) A modulo-12 counter could be used as part of the design of a clock to indicate the hours during the day. How many unique states will you need in the finite state machine (FSM) for the modulo-12 counter, and how many bits do you need *(minimum)* to represent them? (1 mark)

e) You are asked to design the FSM to capture the behaviour of the modulo-12 counter described in part d). Produce a state transition diagram to describe the design, showing all state transitions. The FSM should have a synchronous reset input signal. (5 marks)

[PTO]

f) Assign unique state codes to each state and add these to your completed state transition diagram from part e). (1 mark)

g) Figure 2 provides a module definition for the modulo-12 counter. The design is missing an `always` block to describe the required functionality of the counter. Produce the missing `always` block to describe the operation of the counter. (5 marks)

```
module mod12(input              clock, reset,
             output reg [3:0]   state);

// always block here

endmodule
```

Figure 2

4.

a) Using a suitable diagram explain the concept of the "three box model" when discussing the components of a computer system. Discuss the role of the system bus. (2 marks)

b) Briefly explain why an interface is required between the CPU and an I/O device. (1 mark)

c) What is the main advantage of the use of interrupts over the polling of I/O devices? (2 marks)

d) Produce a simple diagram that illustrates the use of daisy chaining for enabling a simple interrupt priority scheme for three I/O devices. (3 marks)

e) State the order that the following I/O devices should be connected to the CPU using a daisy chaining scheme:

- Scanner (sometimes used)
- External hard disk (used extensively)
- Printer (rarely used)

(1 mark)

f) Figure 3 illustrates the hardware for implementing a parallel priority scheme for four interrupting I/O devices. Briefly explain:

i) the purpose of the mask register (2 marks)
ii) the role of the priority encoder (2 marks)
iii) when IRQ will be raised (1 mark)

g) Table 1 provides the truth table for a priority encoder, and Figure 4 presents a partial Verilog module implementation. Write down the Verilog code for an `always` block that will provide the required functionality for the priority encoder. (6 marks)

[PTO]

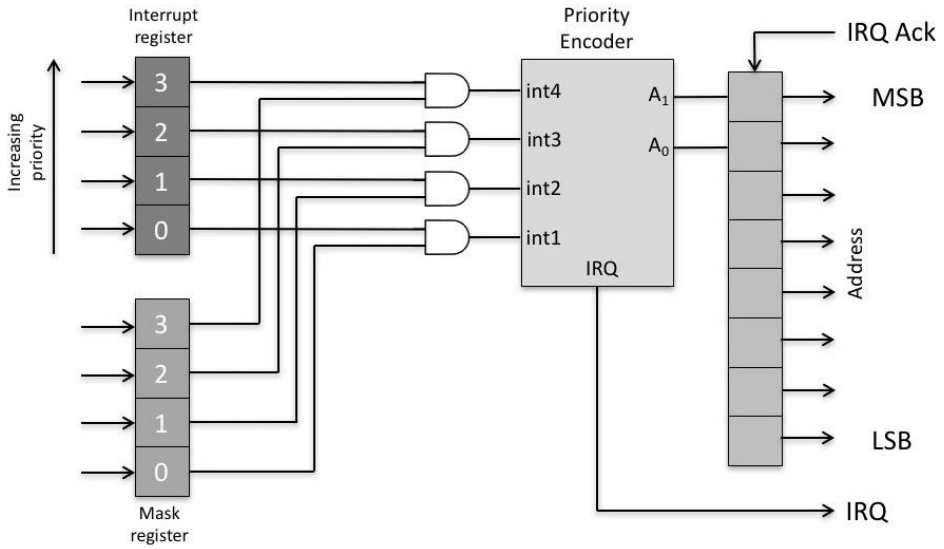

Figure 3

```
module prior_enc(input                int1, int2, int3, int4,
                 output reg [1:0]     address,
                 output reg           irq);

  always @ (*)

      // your code here


endmodule
```

Figure 4

Inputs				Outputs	
int4	int3	int2	int1	irq	address
0	0	0	0	0	XX
0	0	0	1	1	00
0	0	1	X	1	01
0	1	X	X	1	10
1	X	X	X	1	11

Table 1

END OF EXAMINATION