Two hours - online

EXAM PAPER MUST NOT BE REMOVED FROM THE EXAM ROOM

UNIVERSITY OF MANCHESTER
DEPARTMENT OF COMPUTER SCIENCE

Fundamentals of Computer Engineering

Date: Wednesday 15th January 2020

Time: 09:45 - 11:45

This is an online examination. Please answer ALL Questions
The examination is worth a total of 60 marks
The exam contains MULTIPLE CHOICE QUESTIONS

This is a CLOSED book examination

Electronic calculators may be used in accordance with the University regulations

Section A

Section A contains restricted multiple choice questions (MCQs) and is NOT published

Section B

14. For inputs A and B, give the expression for the sum, S, and the carry out, Co, for the half adder. How would you use the half adder to build the 1-bit full adder? In your answer, it is expected that you detail the inputs, connections and final outputs. (3 marks)

15. What is the critical path in a ripple-carry adder? If the delay in one 1-bit full-adder is 36 nanoseconds, what will be the approximate delay for an 11-bit adder? (3 marks)

16. When is a NAND gate True for two independent inputs A and B? When is a NOR gate True, for two independent inputs C and D? Why are NAND and NOR gates referred to as universal gates? (4 marks)

17. Why do we need to use Computer Aided Design (CAD) tools in modern hardware design? (2 marks)

18. What are the four basic signal values that can be displayed in a timing diagram (e.g. like the one you would see in the waveform viewer)? (2 marks)

19. You are a hardware designer and you are asked to produce a complete Verilog module to describe an up-down 4-bit counter with a synchronous reset. The module has a control input "up" which controls its behavior. If up = 1 the counter counts up every clock pulse, of up = 0 then the counter counts down every clock pulse. You should provide a 4-bit output representing the current count. (6 marks)

Section C

20. Describe the three elements of the 3-box model. Outline the contents of the system bus, that connects these three elements. (2 marks)

21. A dynamic RAM (DRAM) memory cell, as illustrated in Figure Q21, consists of a transistor and a capacitor to store a single bit of data. Explain:

    a) how a write operation is performed (3 marks)

    b) how a read operation is performed (3 marks)

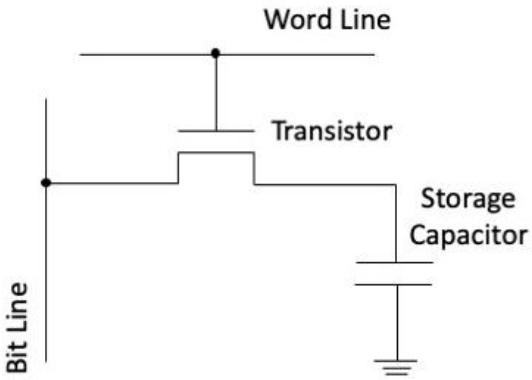

Figure Q21

22. Figure Q22 illustrates the one-dimensional addressing scheme, explain how it can be used to access a particular location in memory. What is a disadvantage of the one-dimensional addressing scheme? (4 marks)

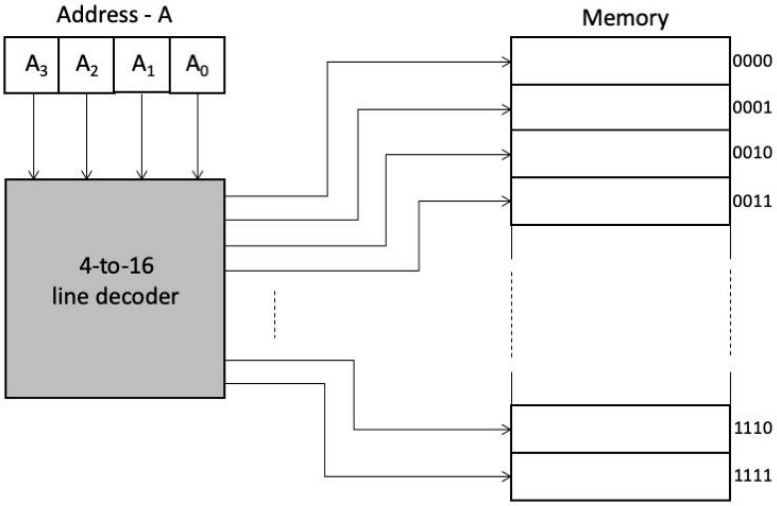

Figure Q22

[PTO]

23. Figure Q23 illustrates an example of a two-dimensional addressing scheme. What advantages does the two-dimensional addressing scheme have over the one-dimensional addressing scheme. (2 marks)

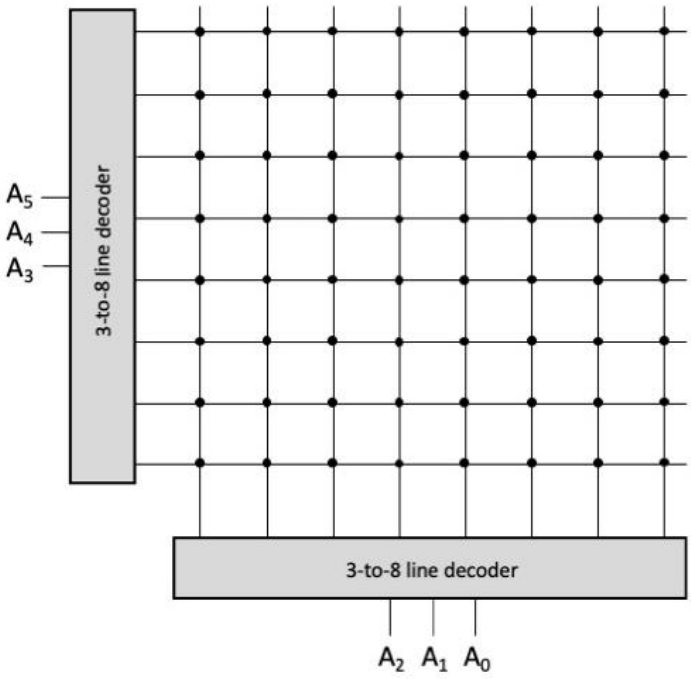

Figure Q23

24. A processor design has a 12-bit data bus and an 8-bit address bus. Suggest suitable size line decoders for a two-dimensional addressing scheme that will allow a memory to support this design. (1 mark)

25. Figure Q25 provides the module outline, including header, for a Verilog module for implementing a 3-to-8 line decoder design. Provide the Verilog code for the always block that will implement the required functionality of the design. (5 marks)

```
module line_decoder(input      [2:0]     address_in,
                    output reg [7:0]     decode_out);

always @ (*)

// your code here


endmodule
```

Figure Q25

END OF EXAMINATION