Two hours - online

Note that the last two pages contain Figures provided for Questions 17, 22a and 22b

UNIVERSITY OF MANCHESTER
DEPARTMENT OF COMPUTER SCIENCE

Processor Microarchitecture

Date: Monday 13th January 2020

Time: 09:45 - 11:45

This is an online examination. Please answer ALL Questions
The examination is worth a total of 60 marks

This is a CLOSED book examination

Electronic calculators may be used in accordance with the University regulations

Section A

1. Show how the use of a *k* stage pipeline can lead to a speed improvement of *k* compared to the unpipelined case. What is meant by a “balanced” pipeline? (3 marks)

2. State two examples of pipeline hazard. What is a common approach that is used to combat the issues associated with pipelining designs? (2 marks)

3. What is the difference between cycle time and latency? As you increase the depth of a pipeline, which should you expect to increase, the cycle time or the latency? (2 marks)

4. Figure Q4 illustrates a block diagram of a self-checking testbench. Identify the elements of the testbench labelled a, b, c and d. (2 marks)

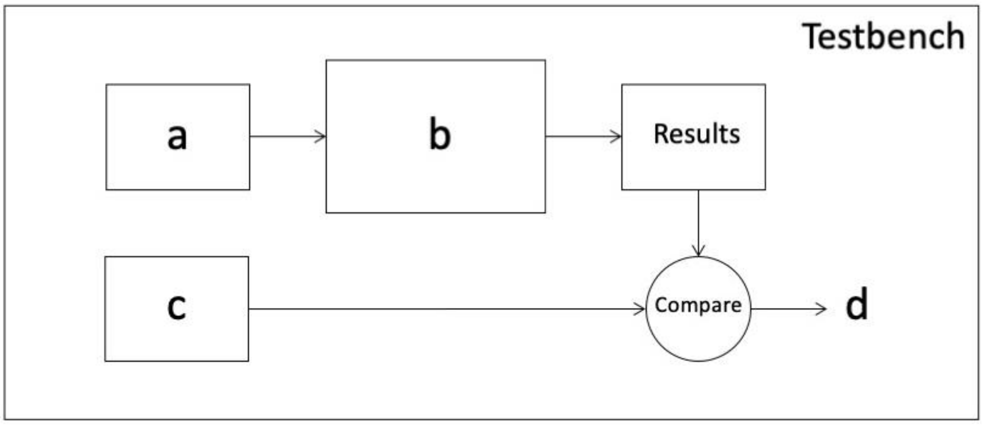

Figure Q4

5. Briefly discuss the difference between unit testing, integration testing and regression testing. Which of the three would normally come first? (1 mark)

Section B

6. Give four different examples of structural blocks that are commonly found in processors and VLSI units. (2 marks)

7. What is meant by the term *Instruction Set Architecture*, or ISA? Give examples of two different commercially successful/contemporary ISAs. (2 marks)

8. Suggest some advantages in having open-source ISAs compared to commercial ISAs. (2 marks)

9. What is a look-up table (LUT)? Why do Field Programmable Gate Arrays (FPGAs) use look-up tables to implement logic in hardware instead of utilising physical logic gates? (2 points)

10. What is a shift register? What is the difference between the bidirectional shifter and the barrel shifter? Hint: explain what each is and how they differ. (2 marks)

[PTO]

Section C

11. What is a floating-point unit and what are some typical operations? You are designing a new processor, suggest some reasons for including/excluding specialised floating-point hardware. (5 marks)

12. What is normalised form? What do we use *normalised* for in floating-point representation? Provide an example. (4 marks)

13. This question aims to test your understanding on converting numbers to floating-point representation. Convert -35.25 to its hexadecimal representation in IEEE floating point single precision representation. (2 marks)

14. This question aims to test your understanding on converting from a floating-point representation. Convert the hex number 0x40200000, in IEEE floating-point single precision representation, to decimal. (2 marks)

15. What is the decimal value for the binary value 1000 1100 0100, where the first 8 bits represent the mantissa/significand and the last 4 bits are the exponent. Hint: the number is given in 2's complement form. (2 marks)

16. Why do we need Machine Learning accelerators? What are the main mathematical operations they are required to perform? What are the main components of a Tensor Processing Unit (TPU)? (5 marks)

Section D

17. Figure Q17 illustrates the RTL datapath of a processor design. Briefly explain how the inclusion of a register bank, reg_bank, satisfies the requirements for a load/store architecture. (1 mark)

18. For the datapath shown in Figure Q17, why are the contents of the PC connected to the address bus, addr, via the multiplexer mux3? (1 mark)

19. For the datapath shown in Figure Q17, what is the purpose of the component add1? When is this used? (2 marks)

20. For the datapath shown in Figure Q17, what is the purpose of the multiplexer, mux1, at the input to the PC register? (1 mark)

21. Produce a Verilog module, called *extender*, to describe the function of the sign extension block, sign_ext, in Figure Q17. (3 marks)

22. Produce a module description for the processor datapath shown in Figure Q17 in structural Verilog.

    A header for the module is provided for you in Figure Q22a (there is no need to replicate this in your answer). To help you with the design a number of module definitions have been provided for you, as listed in Figure Q22b, apart from the sign extender, which you created in answer to the last question. Define any internal variables required for the implementation of the design and use the component and wire names provided in the circuit diagram for your instantiated components and connections between them. (12 marks)

[PTO]

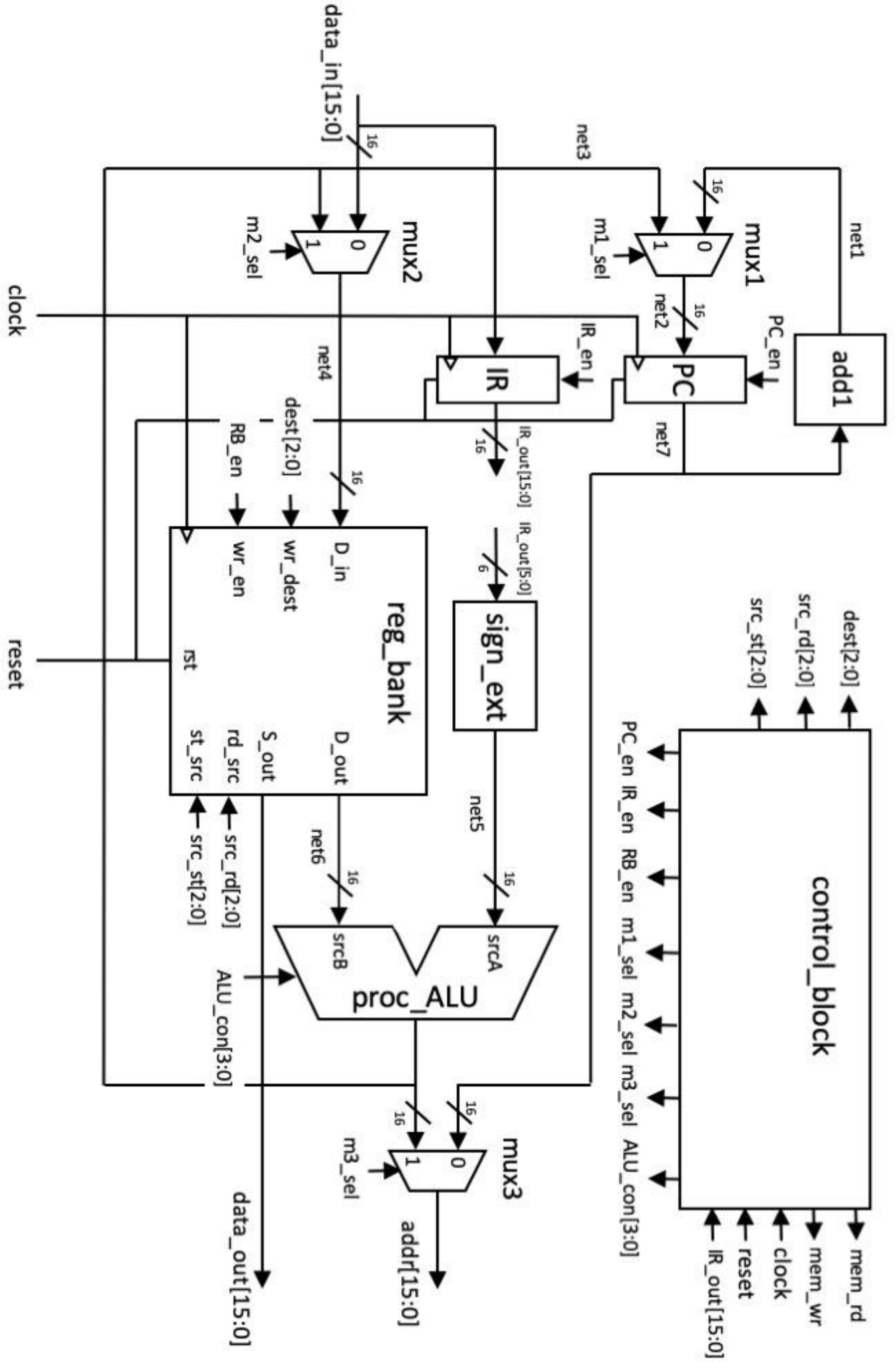

Figure Q17

[PTO]

```
module datapath (input  [15:0]    data_in,
                input           clock, reset,
                input  [2:0]     dest, src_rd, src_st,
                input           PC_en, IR_en, RB_en,
                input           m1_sel, m2_sel, m3_sel,
                input  [3:0]     ALU_con,
                output [15:0]    IR_out, data_out, addr);


// module implementation in structural Verilog


endmodule
```

Figure Q22a

```
module reg_16bit(input       [15:0]  data_in,
                    input             clk, rst, enable,
                       output reg [15:0]  data_out);

module mux_2to1( input      [15:0]   Din0, Din1,
                       input             sel,
                       output reg [15:0]  Dout);

module increment(input      [15:0]  num_in,
                output reg [15:0]  inc_out);

module registers(input      [15:0]  D_in,
                input      [2:0]   wr_dest, rd_src, st_src,
                input             clk, rst, wr_en,
                output reg [15:0]  D_out, S_out);

module ALU(      input      [15:0]  srcA, srcB,
                input      [3:0]   ALU_sel,
                output reg [15:0]  ALU_out);
```

Figure Q22b

END OF EXAMINATION