One and a half hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Digital Systems

Date: Monday 19\textsuperscript{th} May 2008
Time: 14:00 – 15:30

Please answer Question ONE and one other Question

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text.
1. **COMPULSORY**

There are twelve parts to this question. Answer any ten. Typically answers should be one or two sentences. Each part is worth two marks.

a) Why must the pull-up and pull-down networks in CMOS be complementary?

b) Give an equation for the power consumption of a single CMOS gate. For any one of the terms in the equation, explain the practical limitations of using that term to reduce power consumption.

c) What is the threshold voltage of a MOS transistor, and how can it affect propagation delay.

d) The diagram in Figure 1d shows the cross section of an NMOS transistor. What materials are A,B,C, and D made of?

![Figure 1d](image-url)
(Question 1 continues from the previous page)

e) Determine the function of the CMOS logic gate in Figure 1e

![Figure 1e](image)

f) Give two manufacturing factors that limit the minimum size of components in CMOS integrated circuits, stating briefly how they act to limit manufacturable size.

g) Explain why it might be necessary to use a tri-state output device on an address bus.

h) Give two reasons for the desirability of designing complete systems on a single silicon chip.

i) What assumptions must be made if a process pipelined into N stages is to go N times faster?

j) How many unique voltage levels can be output by an 8-bit DAC? What does saying that a DAC is non-monotonic mean?

k) Give two methods of determining interrupt priority.

l) If a cache miss takes 20 times longer than a cache hit and a cache hits 98% of this time, what proportion of the possible processing cycles are wasted?
2. a) Describe the methods by which charge is transported in p and n type doped silicon. (2 marks)

b) Why do the resistivities of p and n type doped silicon differ, and which is larger? (2 marks)

c) In Figure 2, the resistance of transistor $T_1$ is $R_1 \, \Omega$, the resistance of transistor $T_2$ is $R_2 \, \Omega$, and the capacitance of node B is $C$ Farads. Explain how node B charges and discharges when input A changes $1 \rightarrow 0 \rightarrow 1$, and derive expressions for the charging time and discharging time. (3 marks)

![Figure 2](image)

Figure 2

d) Why would it be desirable that the charging and discharging times be similar, and how would $T_1$ and $T_2$ be designed to achieve that? (3 marks)

e) By drawing transistor level circuit diagrams of a 2 input NAND gate and of a 2 input NOR gate, and referring to your answers above, explain why NAND logic is preferred to NOR logic in CMOS. (10 marks)
3. a) Distinguish carefully between the following types of memory devices and give an example of where each might be used in a computer system

   i) Dynamic Random Access Memory
   ii) Serial access Flash EEPROM

   (4 marks)

b) A non-pipelined microprocessor system is on the market. It uses fast but expensive DRAM. The manufacturer wishes to use a cheaper, lower bandwidth memory to cut costs. Explain how pipelining could be used to allow this without a significant loss of performance.

   (7 marks)

c) Serial access Flash EEPROM is used for backup storage in the system. The microprocessor handles all data transfers from the backup memory to main memory. Explain with the aid of a diagram how a Direct Memory Access (DMA) controller could be added to the system and how this would improve the efficiency of this system. Indicate how the DMA controller would need to be initialised when the system is booted.

   (6 marks)

d) The microprocessor bus interface was redesigned to handle the DMA controller by adding a multi-master capability. All buses including the control bus were made tri-state. On testing with the DMA controller it was found that erroneous data was being written to memory. Explain how this could occur and suggest a possible solution.

   (3 marks)