Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Digital Design Techniques

Date: Friday 16th May 2008
Time: 14:00 – 16:00

Please answer any THREE Questions from the FOUR questions provided

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text.
1. a) Explain the effects of CMOS process scaling on:

i) Drain to source current.

ii) Total power consumption on chip.

iii) Gate delay.

You may assume that:

\[ I_{ds} = \frac{\beta (V_{gs} - V_t)^2}{2} \quad 0 < V_{gs} - V_t < V_{ds} \]

\[ \beta = \frac{\mu \varepsilon}{t_{ox}} \frac{W}{L} \]

where the symbols have their usual significance. (6 Marks)

b) A CMOS gate has a gate delay of 0.2ns and is connected to an identical gate by 5mm of 500 nm wide track. The sheet resistance of the track is 0.06 Ohms/square and the track capacitance is 0.1 fF/\( \mu \)m\(^2\). The gate input capacitance is 25 fF. Calculate the ratio of the gate delay to the track delay for the two gates. If the process used to fabricate the gates is scaled down by a factor of 5 but the interconnect stays the same length, calculate the increase in track delay. Hence the new ratio of gate delay to track delay. Comment on the implications of this result for CMOS process scaling. (8 Marks)

c) Describe three ways in which a performance improvement has been made in modern CMOS processing which do not require dimensional scaling. (6 Marks)
2. a) Three different CMOS implementations of the same logic function are given in Figure 1.

i) What is the logic function?

ii) Which implementation uses the least silicon area?

iii) Which is the complex gate implementation?

iv) What is the main disadvantage of the circuit shown in Figure 1 (i) and how might it be overcome? (5 Marks)

![Figure 1](image)

b) Draw a stick diagram of the layout for the implementation shown in Figure 1 (iii) and provide a suitable key to the diagram. (9 Marks)

c) The CMOS NAND gates in Figure 1 (ii) are constructed from n-channel devices with an effective channel resistance of 5k Ohms and p-channel devices with an effective channel resistance of 7k Ohms. Both MOSFETS have an input capacitance of 5 fF and the gate has an unloaded output capacitance of 1 fF. Calculate the worst-case output rise and fall propagation delays for the circuit stating any assumptions made in your calculation. (6 Marks)
3. a) Using a suitable diagram, discuss the control and operation of a $2^n:1$ multiplexer. What two primary functions can a multiplexer be used for? (3 marks)

b) If a multiplexer has $2^n$ data inputs and can implement a function of $k$ variables, what is the maximum value of $k$, without the need for extra logic, if,

i) The input variables are only connected to the multiplexer select inputs?

ii) The input variables are connected to the multiplexer data and select inputs? (2 marks)

c) Multiplexers are often implemented using transmission gates. Using a suitable diagram discuss the operation of a transmission gate. Why is a complementary arrangement of transistors adopted? Using the symbol representation of a transmission gate, show how a 2:1 multiplexer may be implemented using transmission gates and inverters. (6 marks)

d) Implement the following functions using 4:1 multiplexers, illustrate your implementations.

i) $Z = \overline{A}.C + B.C + A.\overline{B}.\overline{C}$, using A and B as the data select inputs

ii) The sum and carry blocks of a full adder, with the Multiplexer data inputs a function of the carry in signal

iii) $Z = \overline{A}.\overline{B}.\overline{C}.\overline{D} + \overline{A}.C.D + \overline{A}.B.C+A.\overline{C}.D+A.\overline{B}.D$ using A and B as the data select inputs. (9 marks)
4. a) The ASM chart illustrated in Figure 2 has a number of errors. Identify the mistakes, stating why they are errors. If the ASM chart were corrected, what type of machine would be implemented? (5 marks)
b) Discuss the disadvantage of the ripple carry adder illustrated in Figure 3. Sketch a modified circuit that will permit both addition and subtraction of 2-s complement binary numbers. How can an overflow condition be detected? (6 marks)

![Figure 3](image.png)

**Figure 3**

(c) Figure 4 illustrates a 4-bit serial adder with accumulator. Briefly describe the operation of this circuit showing the contents of the accumulator and addend register after each clock pulse with the initial contents illustrated? (4 marks)

![Figure 4](image.png)

**Figure 4**

(Question 4 continues on the following page)
d) Figure 5 illustrates the ASM chart describing the operation of the serial adder control circuit. Produce a state table from this ASM chart. You may assume that each state is assigned the state codes illustrated in Figure 5. Using map-entered variables where required, construct two-variable next state and output Karnaugh maps and produce logic equations for their implementation. (5 marks)