Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Digital Design Techniques

Date: Tuesday 26th May 2009

Time: 09:45 – 11:45

Please answer any THREE Questions from the FOUR questions provided

This is a CLOSED book examination

For students attempting Question 3, an additional answer sheet containing a partially completed ASM chart is attached. Hand the completed sheet in at the end of the examination with your answer book.

The use of electronic calculators is permitted provided they are not programmable and do not store text.
1. a) A complex CMOS logic gate is to be designed to produce the logic function:

\[ Q = A \overline{B} + B \overline{A} \]

Explain how the pull-up and pull-down networks are derived from this logic expression and draw a circuit diagram of the gate. It may be assumed that true and compliment values of A and B are available. (6 marks)

b) Explain how stick diagrams help in translating from a circuit diagram to a layout. Use a stick diagram to provide a suitable layout for the gate in Q1.a. (Provide a suitable key for your stick diagram). (6 marks)

c) State the important factors in deciding the final transistor sizes in this circuit. (5 marks)

d) Show that the addition of an inverter on one input a or b is equivalent to adding an inverter to the output of this gate. (3 marks)

2. a) The diagram Figure Q2a) gives a cross section through an inverter implemented using a double well CMOS process. Give the names of the regions labelled A, B and C and state whether the majority carriers in these regions would be holes (p-type doping) or electrons (n-type doping). (3 marks)

![Figure Q2a)](image)

b) What is the purpose of the well contacts? (3 marks)
c) The standard CMOS process is often called a self-aligned gate process. Explain what this means in terms of the fabrication sequence used to produce the transistors.

(3 marks)

d) Explain why the field oxide is much thicker than the gate oxide. Describe how the field oxide is produced in a typical process and why the width of the MOSFET channel is reduced, compared to that on the photomask, during this process stage.

(6 marks)

e) Give three examples of process enhancements in a modern CMOS process which have allowed scaling to lower dimensions.

(3 marks)

f) What is a local interconnect layer and why is it important for producing compact cell designs? Why is it not used for global wiring?

(2 marks)

3. You are required to design a new car park barrier control system for the University staff car park. Entry to the car park is achieved by swiping a valid library card through a card reader at the barrier. If the card is valid, then the barrier should open and stay raised until the car has cleared the barrier, at which point it should then close. The verification of the library card is performed elsewhere, and a signal is provided, C_VALID, that is asserted when a valid card has been swiped. A number of sensors are provided which provide the following input signals for your system:

- C_IN: is asserted when a car has approached the barrier entrance
- C_CL: is asserted when a car is present on the car park side of the barrier
- B_UP: is asserted when the barrier is in the fully raised position, i.e. open
- B_DOWN: is asserted when the barrier is in the down position, i.e. closed

You also have to provide the following control signals to the barrier system that control the opening and closing of the barrier:

- M_UP: is asserted to drive the barrier to the open position
- M_DOWN: is asserted to drive the barrier to the closed position

The design of the barrier control system must ensure that the barrier only opens when a car is present at the entry of the car park and a valid card has been swiped. Once the car has passed through the barrier it must only close once the car has moved under barrier and passed the sensor on the car park side of the barrier, C_CL. The time it takes to raise and lower the barrier is longer than the control system clock period, so you must reside in a state until the barrier has fully opened or fully closed. It is assumed that the barrier is always closed when a car approaches the entrance.

(Question 3 continues on the following page)
(Question 3 continues from the previous page)

a) Figure Q3a) illustrates a partially completed ASM chart showing a Moore design for the required control system. Using the answer sheet provided, complete the design. (6 marks)

b) Use minimum state locus to assign the state vectors to the ASM chart given that the code for the Start state is ‘00’. What is the minimum state locus for your assignment? Produce a state table for your design. (8 marks)

c) Using map-entered variables produce next state maps for the design and produce a circuit schematic of the implementation using 4:1 multiplexers and any additional logic. (6 marks)
4. a) A conventional $n$-bit binary adder can be implemented as illustrated in Figure Q4a). Discuss the disadvantages to this approach with respect to the length of the numbers being added, $n$. Draw a modified circuit, based on the circuit illustrated in Figure Q4a), which will allow two $n$-bit signed numbers to be added. What approach can be adopted to overcome these limitations? (5 marks)

![Figure Q4a)

b) Figure Q4b) illustrates a design for a 4-bit binary multiplier. Discuss, using the numerical example of $1011 \times 0101$, the operation of the multiplier circuit illustrated. Define the operation of the control signals illustrated. (5 marks)

![Figure Q4b)

c) A control system for the multiplier can be designed to have 8 states. Discuss, using the aid of diagrams where necessary, a design which results in a reduced number of states. How many states does your proposed design have? What extra component and control signals are required for your proposed design? (3 marks)

(Question 4 continues on the following page)
(Question 4 continues from the previous page)

**d)** You are required to modify the design of the multiplier in Figure Q4b) to be able to multiply two 4-bit 2’s complement numbers. Produce a diagram of the new signed binary multiplier and discuss the operation of the additional hardware and control signals required in order to perform signed binary multiplication.

(6 marks)

**e)** A binary multiplier can be produced using an iterative network of logic gates and adders, discuss the advantages of this approach over the design proposed in Figure Q4b).

(1 mark)

END OF EXAMINATION

(Of note - see additional answer sheet if attempting Question 3)
Partially completed ASM chart – for use in answering Question 3

StUDENT ID: _________________________