Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

From Transistors to Systems-on-Chip

Date: Friday 5th June 2009
Time: 09:45 – 11:45

Please answer any THREE Questions from the FIVE questions provided

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text
1. a) Answer the following questions about the CMOS pass gate circuit shown in Figure 1, assuming that a high level on Vin, En or En is 1.8V and a low level is 0V.

Transistor thresholds

T1 = + .4V
T2 = - .4V

Minimum sized transistors with W/L = 1/1.

![CMOS pass gate circuit diagram]

**Figure 1**

i) If En is high and Vin = 0V, what is the output voltage level and identify which, if any, transistor(s) is/are on. (2 marks)

ii) If En is high and Vin = 1.8V, what is the output voltage level, and identify which, if any, transistor(s) is/are on. (2 marks)

iii) Are the rise and fall times at Vout the same? If different, explain why this arises and identify the longer. (3 marks)

iv) Explain what happens to the voltage level at Vout when En is taken low. Hence, draw a truth table and state what logic function the CMOS pass gate is performing. (3 marks)

v) With the aid of a diagram, show how two CMOS pass gates can form a 2-to-1 multiplexer and briefly explain its operation. (2 marks)

b) With the aid of a diagram, describe how the logic in part a(iv) and a(v) can be used in providing a double edge triggered flip flop. (5 marks)

c) Discuss why a double edge triggered flip flop is a useful function and the advantages that the implementation in part (b) has over an implementation in conventional CMOS circuitry. (3 marks)
2. This question refers to the clocked dynamic logic gate shown in Figure 2.

**Figure 2**

\[
\text{Vs} = 1.8V \\
\text{T3} \quad \text{Vtp} = -0.4V \\
\text{OUT} \\
\text{DATA} \\
\text{T2} \\
\text{X} \quad \text{Vtn} = 0.4V \\
\text{T1} \\
\text{OV}
\]

a) Explain the operation of the circuit and aid your explanation with a timing diagram. (4 marks)

b) If Enable = 0V and Data = 1.8V
   i) Which transistors are on and which are off? (4 marks)
   ii) What are the voltage levels at Out and X? (4 marks)

c) If following Enable = 0V and Data = 0V, Enable changes to 1.8V, what voltage would be expected at Out and what (if anything) would happen at Out if Enable were left permanently at 1.8V? (3 marks)

d) Explain why the Enable signal is connected to transistor T1 rather than T2. Aid your answer by considering what happens to the voltage at Out if the Enable is connected to T2, Data to T1 and the capacitance at Out is four times that at point X. (6 marks)

e) This logic is also called Domino Logic. Explain why this is so and explain how the output Out must be connected to succeeding gates. (3 marks)
3. a) Outline the reasons for including a cache memory in a processor design. (2 marks)

b) Draw a block diagram of a cache memory and explain its operation. (4 marks)

c) Figure 3 shows the circuit of a content addressable memory cell (CAM). Explain carefully how the cell reads, writes and associates. (7 marks)

d) Describe how a wire-or connection can be used across a row of CAM cells to indicate whether or not particular data is held by the row. (2 marks)

e) Conventional static random access memory cells (SRAM) normally forms the data part of a cache memory.

i) Sketch a typical SRAM cell.

ii) By comparing the number of transistors in the SRAM cell and CAM cell, estimate the difference in area of the two cells.

iii) SRAM cells incorporated into SRAM memories require address decoders plus read circuits and write circuits. Are all these required in a cache memory implementation? (5 marks)
4. a) Why do adders in most systems accelerate the carry? (2 marks)

b) Explain the principle of a Carry Look Ahead (CLA) adder. (4 marks)

c) Why is the group size in a CLA often chosen to be 4? (2 marks)

d) Assuming a group size of 4 and an adder length of 32-bits for the remaining sections of the question, explain how the CLA principle can be extended over groups of groups. Aid your description with an appropriate diagram. (5 marks)

e) Assuming a groups of groups organization for the 32-bit CLA adder, show schematically the carry path into the most significant bit of the adder (i.e. C_{31}). (4 marks)

f) If the operation time for a logic stage is \( t_d \), estimate the addition time of your groups of groups 32-bit CLA adder. (3 marks)

5. a) Give a block diagram of the logic for a simple bit-by-bit multiplier and describe its operation. (5 marks)

b) Explain how this multiplier multiplies by negative numbers. (2 marks)

c) The multiplication speed can be improved by interpreting the multiplier bits i-bits at a time as a signed number. If \( i \) is one bit (original Booth's algorithm), give a table to show the operations that this causes in the multiplier for a current multiplier bit of '0' and a current multiplier bit of '1'. (2 marks)

d) Give a multiplier pattern where:

i) original Booth's algorithm generates fewer sub-products than the simple multiplier;

ii) original Booth's algorithm generates more sub-products than the simple multiplier.

In both cases explain how this arises. (4 marks)

e) Explain how the original Booth's algorithm can be modified by considering the multiplier bits in signed pairs (\( i=2 \)). (4 marks)

f) Discuss why although \( i \) can be greater than two, this is usually an unattractive option. (3 marks)

END OF EXAMINATION