Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Systems Architecture

Date: Friday 21st May 2010
Time: 14.00 – 16.00

Please answer THREE Questions from the FOUR questions provided

Use a SEPARATE answerbook for each SECTION

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text.
Section A

1. a) Explain why a modern processor often has separate instruction and data caches. (2 marks)

b) Why do most modern processors have at least two levels of cache? (2 marks)

c) Explain what is meant by the terms ‘write back’ and ‘write through’ in the context of write operations to data in a cache. Discuss the advantages and disadvantages of each approach. (4 marks)

d) Explain what is meant by a ‘cache line size’ and discuss the influence of the line size on the performance of the cache. (4 marks)

e) A direct mapped cache stores 8 kbytes of data and has a line size of 32 bytes. It is used in a processor which uses a 32 bit address and data word, and can access memory at an 8 bit byte level.

i) Sketch the structure of the cache and the way in which the address is used to access the data. (4 marks)

ii) If the cache is initially empty and the following sequence of read addresses are generated by the CPU, which of the accesses result in a cache miss and why? (4 marks)

0x00000000
0x00000020
0x00000040
0x00000060
0x00000028
0x00000050
0x00000080
0x00000098
2. a) Explain how pipelining can reduce the execution time of a serial stream of instructions. (2 marks)

b) With the aid of a diagram, explain the operation of each of the stages of a classic 5 stage pipeline. (4 marks)

c) Explain why branches cause problems for pipelines and show what happens to a 5 stage pipeline without branch prediction when the direction of a conditional branch cannot be resolved until the execute stage. (4 marks)

d) With the aid of a diagram, describe how a branch target buffer can be used to alleviate the problems caused by branches. (4 marks)

e) The following sequence of instructions is executed in a 5 stage pipeline. Show the forwarding paths which are required to ensure that the pipeline does not need to be stalled because of data hazards. You may find it useful to draw a timing diagram showing the progress of each instruction through the pipeline. (6 marks)

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LDR R1,x
MUL R2,R2,R2
ADD R0,R1,R2
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3. a) What is “Multithreading” in the context of CPU design? (NB: NOT in the design of software!) (2 marks)

b) Why is Multithreading used in the design of many modern CPUs? (2 marks)

c) What does each of the following terms mean:
   
i) Coarse-grain multithreading? (2 marks)
   ii) Fine-grain multithreading? (2 marks)
   iii) Simultaneous multithreading? (2 marks)

A RISC CPU is running at a clock rate of 1 gigahertz, and can issue one instruction per clock, with no pipeline delays in the best case (100% cache hits; 100% branch predict success, etc). There is only one level of data cache provided, and the CPU implements 2 threads, with a thread switch only on a cache miss.

d) What simplifying assumptions would you make when estimating pipeline throughput? (4 marks)

e) In a particular program, one instruction in 5 reads a memory location – there are no writes. If the main memory has an effective access time of 50 nanoseconds, what is the pipeline throughput at 0.1% cache miss rate? (3 marks)

f) What is the pipeline throughput at 10% cache miss rate? (3 marks)
4. a) What is the difference between Process Virtualization and System Virtualization? (4 marks)

b) What are the major benefits of System Virtualization? (4 marks)

c) Describe how System Virtualization can be implemented on a CPU which provides only two levels of privilege and protection. Outline the level transitions which occur during an application system call (such as GetProcessID) and its return. (6 marks)

d) i) Describe two different debug features you would like to see in an Operating System debugger. (2 marks)

ii) How would you use System Virtualization to implement each of these features? (2 x 2 marks)