Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

From Transistors to Systems-on-Chip

Date: Tuesday 25th May 2010
Time: 09.45 – 11.45

Please answer any THREE Questions from the FIVE questions provided
This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text
1. a) Describe how a NMOS transistor can be used to pass a high and a low voltage level. In each case, indicate which terminal acts as the source and the direction of current flow through the transistor. (6 marks)

b) Explain why the body effect makes a difference to the high voltage level passed. (4 marks)

c) If the supply voltage is 1.8V, the NMOS threshold voltage is 0.4V at a $V_{sb} = 0V$, estimate the high voltage output from the NMOS pass transistor taking the body effect into account. State any assumptions made. (4 marks)

d) If three NMOS pass transistors are connected in series and a supply voltage of 1.8V is input to the chain, indicate the voltage you would expect to see at each point down the chain. (3 marks)

e) If the high level is passed through the series chain of part (d) and the transistors are then turned off, describe what will happen to the voltage at the chain output. (3 marks)

2. a) What are the three sources of power dissipation in a conventional CMOS circuit and what governs their magnitudes? (7 marks)

b) Show that parallelism by a factor of N can be used to reduce power dissipation while maintaining overall performance. (5 marks)

c) Discuss measures that can be taken at the circuit, logic, RTL, architecture and algorithmic levels to minimise power dissipation. (8 marks)
3. a) Give a block diagram of the logic for a simple bit-by-bit multiplier and describe its operation. (5 marks)

b) Explain how this multiplier multiplies by negative numbers. (2 marks)

c) The multiplication speed can be improved by interpreting the multiplier bits i-bits at a time as a signed number. If i is one bit (original Booth's algorithm), give a table to show the operations that this causes in the multiplier for a current multiplier bit of '0' and a current multiplier bit of '1'. (2 marks)

d) Give a multiplier pattern where:

i) original Booth's algorithm generates fewer sub-products than the simple multiplier;

ii) original Booth's algorithm generates more sub-products than the simple multiplier.

In both cases explain how this arises. (4 marks)

e) Explain how the original Booth's algorithm can be modified by considering the multiplier bits in signed pairs (i=2). (4 marks)

f) Discuss why although i can be greater than two, this is usually an unattractive option. (3 marks)
4. a) Briefly explain the principle of operation of a conditional sum adder. 
   (2 marks)

b) Compute the block level conditional sum and carries for such an adder using the block size of one with 8-bit input vectors of 01110111 and 11000011 and an initial carry-in of 0. You should show each level of the evaluation. 
   (8 marks)

c) Discuss the distribution of the longest carry chain length that you might find in an adder used in a general purpose processor. 
   (4 marks)

d) The following diagram shows a fragment of a self-timed ALU. Explain its operation with the aid of Boolean equations, showing how the various outputs are derived.

![Diagram of a self-timed ALU]

\[ *= \text{precharged} \] 

(6 marks)
5. Solid State Disks (SSDs) are increasingly being offered as an option in high-end laptops and servers.

a) Discuss the advantages and disadvantages of SSDs over conventional rotating magnetic disc storage systems. (5 marks)

b) Briefly describe the operation of the basic cell of a flash device. (3 marks)

c) USB memory sticks are relatively slow compared with SSDs, yet the basic technology is similar. Explain how SSDs gain their speed advantages. (2 marks)

d) Outline the architecture of a large capacity SSD. (5 marks)

e) Explain why deleting files on an SSD is problematic and can lead to the phenomenon known as "stuttering". (5 marks)