Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Implementing System-on-Chip Designs

Date: Wednesday 25th May 2011
Time: 09:45 - 11:45

Please answer Question 1 and TWO other questions from the FOUR questions provided

This is a CLOSED book examination

The use of electronic calculators is NOT permitted
Section A

This question is compulsory
Answer any ten of the subsections.
Each subsection carries 2 marks.

1. a) Briefly describe the function of two different types of timing checking CAD tools used in ASIC design. (2 marks)

b) What is the result of simulating a single active edge on the following behavioural Verilog? (2 marks)

```verilog
always @ (posedge clk)
begin
  a <= b;
  b = a;
end
```

c) Explain the significance of regression testing in SoC design. (2 marks)

d) Delays are easy to insert in behavioural Verilog; why can these not be translated into an implementation? (2 marks)

e) What is “Monte Carlo” simulation? Suggest an appropriate application. (2 marks)

f) Briefly explain either one advantage or one disadvantage of a GALS on-chip network. (2 marks)

g) Give two major sources of inaccuracy when simulating a system at the circuit level. (2 marks)

h) What are the two main sources of environmental variation for systems on a chip and how do they affect circuit performance? (2 marks)

i) Distinguish between validation and verification when applied to the design of a system. (2 marks)

j) A low power CMOS multiprocessor chip has the ability to power down sections not in use. The table below shows the total current drain as different areas of the
chip are forcibly powered up in the steady state (no gates switching). The relative size of areas in terms of approximate gate count is also given. If the mean leakage per gate is 20 pA would this chip be rejected on test and if so why? (2 marks)

<table>
<thead>
<tr>
<th>Chip Area</th>
<th>No. of Gates</th>
<th>Current Drain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache/controller</td>
<td>20,000</td>
<td>0.52 µA</td>
</tr>
<tr>
<td>Core 1</td>
<td>50,000</td>
<td>1.15 µA</td>
</tr>
<tr>
<td>Core 2</td>
<td>50,000</td>
<td>8.7 µA</td>
</tr>
<tr>
<td>I/O control</td>
<td>10,000</td>
<td>0.27 µA</td>
</tr>
<tr>
<td>DMA control</td>
<td>10,000</td>
<td>0.26 µA</td>
</tr>
</tbody>
</table>

k) Give two limiting factors which make it difficult to continue to reduce transistor sizes. (2 marks)

l) Why is it necessary to have the actual chip layout for critical timing analysis? (2 marks)
Section B

Answer two questions from this section.

2. On-chip clocks may have frequencies which exceed 1 GHz. Clock signals are typically sourced from an oscillator in the 1 MHz - 32 MHz range.

   a) Why is a synchronous timing model useful in SoC design? (2 marks)

   b) How is synchronous operation guaranteed when implementing an ASIC? (4 marks)

   c) Why are high-frequency clock signals produced on-chip? (2 marks)

   d) How are high-frequency clock signals produced on-chip?
      (A figure or brief description of a mechanism is appropriate.) (4 marks)

   e) What problem is faced when transferring data between unsynchronised blocks on a chip? (3 marks)

   f) Show, using Verilog or a schematic diagram, how this problem may be alleviated. (3 marks)

   g) Comment on the reliability of transferring data between asynchronous regions. (2 marks)
3. [There is no need for knowledge of any specific algorithms in this question.]

Imagine you are tasked to develop an SoC to decode and display a stream of compressed, encoded, high-definition (1920 x 1080) video. The data stream may contain other information in addition to the pixel data.

a) Making (and stating) reasonable assumptions about other display parameters estimate the pixel data rate.

(Answers within an order of magnitude are acceptable.) (2 marks)

b) Suggest two ‘extra’ features which may be processed appropriately in software at the decoder. In each case estimate the bandwidth they may require. (4 marks)

c) Why must the decoder be capable of processing slightly faster than the nominal data rate? (2 marks)

d) Describe two complementary techniques by which parallelism can be employed in the system architecture to meet the required processing rate. In each case explain why the techniques are suitable for this job and outline any costs above a simple serial implementation. (8 marks)

e) Outline two distinct ways in which parallelism is expressed in synthesizable Verilog. State how/if these would be applicable to your answers to part d, above. (4 marks)
4. a) What is meant by the terms *Controllability* and *Observability* when applied to the testing of a logic system? (2 marks)

b) Describe how a complex system may have the controllability and observability of its internal functional blocks improved using the boundary scan technique whilst maintaining a low external pin count. (4 marks)

c) Show using a schematic diagram or otherwise how a JTAG port could be used to simplify access to a system using functional blocks which use the boundary scan technique for testing. (8 marks)

d) Explain how the JTAG standard allows for:
   
   i) Rapid data input to specific function blocks (1 mark)
   ii) Additional testing of some blocks using built in self test for example. (1 mark)

e) The TAP controller for a JTAG port has a sixteen state finite state machine. Why is it necessary to have so many states (a detailed description of actual states is not required). (4 marks)
5. a) Describe the stages in the hierarchy of the design process for a System on Chip going from system specification to final implementation. (8 marks)

b) Discuss the simulation tools used at each step with particular reference to their limitations. (8 marks)

c) How does the use of standard cells for the final layout improve the accuracy of simulation at the higher levels of abstraction and why is back annotation still required for critical timing analysis? (4 marks)