Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Implementing System-on-Chip Designs

Date: Wednesday 6th June 2012
Time: 09:45 - 11:45

Please answer Question 1 and TWO other questions from the FOUR questions provided

This is a CLOSED book examination

The use of electronic calculators is NOT permitted
Section A

This question is compulsory
Answer any ten of the subsections.
Each subsection carries 2 marks.

1. a) Give a brief description of the function of a static timing analyser. (2 marks)

b) In the context of D-type flip-flops, explain what is meant by:
   i) data setup time (1 mark)
   ii) data hold time (1 mark)

c) Some Verilog statements are not, in general, synthesisable. Explain why the ‘initial’ statement can be synthesised for an FPGA but not an ASIC. (2 marks)

d) Why might a designer be content with less than 100% test coverage at a functional level? Give an example of something which may be safely left ‘untested’. (2 marks)

e) Verilog has two ‘equality’ tests: ‘==’ and ‘===’; say how these differ, noting what states can each return. (2 marks)

f) Why is minimising clock skew during layout (place and route) essential in making a working ASIC? (2 marks)

g) What is meant by the terms Controllability and Observability when applied to the testing of a logic system? (2 marks)

h) Explain how the JTAG standard allows for:
   i) Rapid data input to specific function blocks (1 mark)
   ii) Additional testing of some blocks using built in self test for example. (1 mark)

i) Briefly explain why circuit level simulation is required and what the advantages of mixed mode simulation are for SoC designs? (2 marks)

j) Three different CMOS implementations of the same logic function are given in figure 1.
i) What is the logic function for the implementations?

ii) Which implementation uses the least silicon area?

iii) Which is the complex gate implementation?

iv) What is the main disadvantage of the circuit shown in figure 1(i) and how might it be overcome? (2 marks)

Figure 1:

k) Giving your reasons state which of the gate circuits in figure 2 is incorrect? (2 marks)

Figure 2:

l) A process line produces device parameter variations which follow a Gaussian curve. A device costs 20p to fabricate and 1,000,000 devices are produced in a full working day. What is the cost difference per day of changing from a 2$\sigma$ to a 3$\sigma$ rejection threshold? You may assume that the area under a Gaussian curve outside 2$\sigma$ is 4.56% of the total area and outside 3$\sigma$ is 0.26% of the total. Where $\sigma$ is the standard deviation. (2 marks)
Section B

Answer two questions from this section.

2. You are required to create a Verilog module containing a memory model. This is to be used to check a processor design which is to be tested. The specification is for a 4 Kbyte memory with separate 32-bit input and output data buses.

   a) Sketch out the basic code to implement the memory module including the interface definition. [Concentrate on the operation; minor syntactic errors are not important.]

   (4 marks)

   b) The processor being tested needs to run code from this memory; how could the memory contents be set up?

   (2 marks)

   c) For testing purposes the model should check that the address and write data buses remain stable throughout a write operation. Suggest how any violations of this condition may be detected and reported.

   (2 marks)

   d) To provide a more realistic model, when reading the memory it is desired that the data out is undefined for 50 time units following an address change before adopting the proper value. Show how you could achieve this by adding to or adapting your previous model.

   (4 marks)

   e) The memory system is to be extended to use N of your modules, where ‘N’ is a power of two passed to the code as a parameter. Without modifying the basic module, using code if necessary, describe how this can be done. Make it clear where connections would go and if any other support logic is needed.

   (8 marks)
3. a) Sketch a timing diagram for a read and a write cycle on a simple, asynchronous peripheral bus. Ensure that the sequence of signal switching is clear. (4 marks)

b) Explain why bidirectional signals are rarely, if ever, used in systems on chip with modern manufacturing processes. (3 marks)

The AXI bus passes signals synchronously along pipelines between D-type registers. The control ‘handshake’ protocol has two signals: a forward-going valid which indicates the presence of data and a backward-going ready which indicates a stage is ready to receive new data. Both control signals are output from latches and changes are synchronised with data changes.

c) Under what conditions is data transferred between AXI stages? (1 mark)

d) Explain why, in a minimum hardware AXI implementation, no more than half the stages can contain valid data. (4 marks)

e) How can the minimal design described in the previous section be adapted(expanded) to provide better throughput? (3 marks)

f) Employing a bus like AXI is done to give a ‘higher performance’ than a simpler bus. Explain why this can be achieved this in the case of operations such as cache fills. (3 marks)

g) Suggest a type of operation which might be slower on an AXI bus than a simpler protocol; why might this be the case? (2 marks)
4. a) A complex CMOS logic gate is to be designed to produce the logic function:

\[ Q = A\overline{B} + B\overline{A} \]

Explain how the pull-up and pull-down networks are derived from this logic expression and draw a circuit diagram of the gate. It may be assumed that true and complement values of A and B are available as inputs. (6 marks)

b) Explain how stick diagrams help in translating from a circuit diagram to a layout and use a stick diagram to provide a suitable layout for the gate. (Provide a suitable key for your stick diagram). (6 marks)

c) State the important factors in deciding the final transistor sizes in this circuit. (5 marks)

d) Show that the addition of an inverter on one input A or B is equivalent to adding an inverter to the output of this gate. (3 marks)

5. a) Discuss the major limiting factors which make continued scaling of CMOS devices to smaller dimensions difficult. (8 marks)

b) Sketch the generalised curve representing the failure rate for a CMOS device during its lifetime and explain the effect of scaling a system to smaller dimensions on this curve. (3 marks)

c) Give three technology innovations that have been used to allow the scaling of CMOS to the dimensions used in modern SoC devices. For each innovation discuss the effects of further reduction in size particularly with regard to device reliability. (3 * 3 marks)