Implementing System-on-Chip Designs

Date: Wednesday 22nd May 2013
Time: 09:45 - 11:45

Please answer Question 1 and also TWO other questions from the remaining FOUR Questions provided

This is a CLOSED book examination

The use of electronic calculators is NOT permitted

[PTO]
Section A

This question is compulsory.
Answer any ten of the subsections.
Each subsection carries two marks.

1. a) Explain what is meant by “clock jitter”. (1 mark)
How must it be taken into consideration in timing analysis? (1 mark)

b) Draw the truth table for a two input AND gate which processes the Verilog states {0, 1, X}. (2 marks)

c) State two properties where a digital ‘switch-level’ circuit simulator has advantages over a more sophisticated analogue circuit simulation. (2 marks)

d) A particular video camera has a resolution of 1280 x 720 pixels, each pixel requiring 16 bits (2 bytes) of storage. This is streamed, uncompressed, to a framestore at 50 frames/second. Estimate the memory bandwidth required, making clear what units you have used. (2 marks)

Your answer need not be exact; a close estimate is sufficient.

e) Describe the operation of a data transfer using a handshake between two synchronous blocks using the same clock. Make it clear which block \{sender, receiver\} asserts which signal(s) and when. (2 marks)

f) Explain what regression tests are for and when they are used in SoC development. (2 marks)

g) Why is it necessary to have the actual chip layout for critical timing analysis? (2 marks)

h) The standard CMOS process is often called a self-aligned gate process. Explain what this means in terms of the fabrication sequence used to produce the transistors. (2 marks)

i) Explain what is meant by the term ASIC and, giving a suitable example, explain why such parts are economically viable. (2 marks)
j) Describe two limiting factors which make it difficult to continue to reduce transistor sizes in modern System on Chip (SoC) devices. (2 marks)

k) Describe two potential reasons for the failure of CMOS devices in the field. (2 marks)

l) Give two reasons why copper interconnect is preferred to aluminium in modern CMOS SoC devices. (2 marks)
Section B

Answer any two questions from this section.

2. a) What determines the maximum clock frequency at which a synchronous block of logic can be clocked? (2 marks)

b) Briefly describe the operation of a tool to find an estimate of the maximum clock frequency where the run time of the tool is practical even for large circuits. (3 marks)

c) With respect to a register made of D-type flip-flops, define what is meant by:
   • Propagation delay? (1 mark)
   • Data set-up time? (1 mark)
   • Data hold time? (1 mark)

d) Any of the three times above can cause timing problems if violated. Which time cannot be alleviated by reducing the clock frequency – and why not? How can this problem be rectified? (4 marks)

e) Give two different reasons why might it be desirable to build an SoC with several synchronous blocks which have different clocks? (4 marks)

f) If communicating blocks use unsynchronised clocks, what problem may afflict input flip-flops? What is typically done to alleviate this problem? (4 marks)
3. A chip is required for a real-time signal processing task. Part of this involves performing a 32-point Fast Fourier Transform (FFT) on input samples arriving at a rate of 100 million samples/s. The chip is to be clocked at 100 MHz internally as well.

Each set of 32 samples is processed independently so any sample is used in only one transform; all samples are used.

(For the purpose of this question, you can assume that an N point FFT requires $N \cdot \log_2 N$ multiplications.)

*Sensible, appropriate approximations – if necessary – in the arithmetic will be allowed.*

a) How many multiplication operations are required:

- per FFT? (1 mark)
- per second? (1 mark)

b) An iterative multiplier design – which will run at the relevant clock rate – is available. This requires 10 cycles to perform each multiplication. How many multiplications per second is each one capable of? (2 marks)

c) In the context of this problem, suggest a microarchitecture for a ‘better’ multiplier. Justify your choice. Comment on any implications for the design criteria such as speed, area and power consumption. (6 marks)

d) If your ‘improved’ multiplier is still not fast enough, what can you do to meet the processing requirement for this SoC? *Quantify* your answer. (2 marks)

e) Assuming the FFT processor has met its processing specification, there will be 100 million output coefficients generated per second. These are to be written to a RAM buffer from where they will be read out at a similar rate – again all in real-time. The only RAM blocks available of adequate size have a cycle time of 20 ns. Describe how you could use these to fulfill the specification, highlighting the particular problems and techniques you might employ. (8 marks)
4. a) What is meant by the statement that System on Chip (SoC) devices lack Controllability and Observability when referring to testing the system? (2 marks)

b) Describe how a SoC device may have the controllability and observability of its internal functional blocks improved using the boundary scan technique whilst maintaining a low external pin count. (4 marks)

c) Show using a schematic diagram or otherwise how a JTAG port could be used to simplify access to a SoC device using functional blocks which use the boundary scan technique for testing. (8 marks)

d) Explain how the JTAG standard allows for:
   i) Rapid data input to specific function blocks
   ii) Additional testing of some blocks using built in self test, for example. (2 marks)

e) The TAP controller for a JTAG port has a sixteen state finite state machine. Why is it necessary to have so many states (a detailed description of actual states is not required)? (4 marks)
5. a) A complex CMOS logic gate is to be designed to produce the logic function:

\[ Q = \overline{A}.C + B.D \]

Explain how the pull-up and pull-down networks are derived from this logic expression and draw a circuit diagram of the gate.  

(6 marks)

b) How do stick diagrams help in translating from a circuit diagram to a layout? Use stick diagrams to provide a suitable layout for the gate in Q5(a).  
(Provide a suitable key for your stick diagram).  

(6 marks)

c) Describe the important factors in deciding the final transistor sizes in this circuit.  

(6 marks)

d) Show that the addition of two inverters allows this gate to provide the exclusive OR operation:

\[ Q = X.Y + \overline{X}.Y \]

(2 marks)