Implementing System-on-Chip Designs

Date: Friday 30th May 2014
Time: 14:00 - 16:00

Please answer Question 1 and also TWO other questions from the remaining FOUR Questions provided

This is a CLOSED book examination

The use of electronic calculators is NOT permitted
Section A

This question is compulsory.
Answer any ten of the subsections.
Each subsection carries two marks.

1. a) Give two reasons why it is currently sensible to design synchronous circuits, as far as is possible. (2 marks)

   b) In Verilog a signal’s value may be treated as ‘X’. Give two, different interpretations of this value in a Verilog design/simulation/synthesis environment. (2 marks)

   c) What are the variables’ values after the following fragment of Verilog is run? (It can be assumed that \(a\) and \(b\) are large enough not to overflow.) (2 marks)

   ```verilog
   initial
      begin
         a = 5;
         b = 2;
         b <= b + a;
         a <= a + b;
         a = a - 1;
      end
   ```

   d) Sketch a transmission gate and briefly explain how it operates. (2 marks)

   e) What might cause a flip-flop on an input signal of one SoC block to go metastable? (2 marks)

   f) Give two reasons why the supply voltage to the core of a silicon chip has been reduced over the past decade. (2 marks)

   g) Explain what is meant by “time stealing” in a processing pipeline. (2 marks)

   h) Post-layout back annotation is usually used in simulation in an ASIC design flow.

      (i) What is it? (2 marks)

      (ii) Why is it used? (2 marks)

   i) Briefly outline the characteristics of standard cells used in ASIC layout. (2 marks)
j) Why might an ASIC manufacturer’s gate library contain a range of (for instance) two input NAND gates rather than a single example? (2 marks)

k) When simulating the timing of a synthesized circuit the same functional test vectors are applied whilst varying other parameters in the simulation. What are these parameters and why is this done? (2 marks)

l) Draw the truth table for the circuit in figure 1. (2 marks)

Figure 1:
Answer any *two* questions from this section.

2. a) Give examples of appropriate uses of the following types of Verilog variables:
   - (i) wire
   - (ii) reg
   - (iii) int

   (6 marks)

b) The following Verilog statement is supposed to be synthesized into a combinatorial circuit. What is the misconception here and how should it be corrected?

   ```verilog
case (aa[1:0])
   0: y = 3;
   1: y = 0;
   2: y = aa;
endcase
```

(3 marks)

c) Figure 2 shows a simple circuit schematic. Express the same function in Verilog making the code as clear as you can.

![Circuit Diagram]

(3 marks)

d) The following code describes a small FSM; rewrite it with identical functional behaviour so that all its outputs are registered.

```verilog
module demo (input wire clk, input wire reset, output wire zero, output reg lots);

reg [1:0] state;

always @ (posedge clk)
   if (reset) state <= 0;
   else state <= state + 1;

assign zero = (state == 2'b00);

always @ (state)
   if (state == 2'b11) lots = 1;
   else lots = 0;
endmodule
```

(6 marks)

e) State a possible advantage to having registered outputs on a FSM.

(2 marks)
3. a) What is meant by the terms “static” and “dynamic” power dissipation, respectively. 

(2 marks)

b) Describe the various mechanisms by which power is dissipated on a CMOS device. In each case state whether the dissipation is static or dynamic. 

(8 marks)

c) Describe a mechanism which may be employed to:

(i) reduce dynamic dissipation in an FSM when it is not in active use;
(ii) reduce static dissipation in a combinatorial circuit when it is not in active use. 

(4 marks)

d) A SoC dissipates an average of 10 W whilst active and 100 mW when inactive. The core power supply is 1.25 V. There is no appreciable load on the output pins. Calculate the supply current in its active and passive states. 

(2 marks)

e) If the supply voltage can be reduced to 1.0 V without compromising the clock frequency estimate the active and passive dissipation, clearly stating any assumptions and approximations you make. 

(4 marks)
4. a) Sketch a vertical cross-section through a MOS transistor, labelling the features. (2 marks)

b) Describe the switching characteristics of the types of MOS transistor used in a modern digital VLSI chip. Why are Complementary transistors used in CMOS gates? (4 marks)

c) Explain why all basic CMOS gates perform inverting logic functions such as NAND and NOR. (2 marks)

d) Figure 3 depicts a complex CMOS gate. Describe the Boolean function which it implements, e.g. by drawing the clearly labelled corresponding gate symbol. (6 marks)

![Figure 3: Complex CMOS Gate](image)

In figure 3 the PMOS transistor connected to input ‘E’ has a width of $20\lambda$. It is desirable that the gate switches its output with roughly equal rise and fall times. Three other transistors are labelled: state what their widths \{x, y, z\} should be, in each case justifying your answer. (6 marks)
5. a) What does “yield” mean when silicon chips are manufactured? How is it determined in practice? (2 marks)

b) What causes the *yield* to be less than 100%? (2 marks)

c) In what way(s) do production tests differ from tests used in design verification? (4 marks)

d) What is meant by “controllability” and “observability” in testing? State to what type of tests are these applied and why? (4 marks)

e) Why are sufficient *controllability* and *observability* difficult to achieve from the periphery of a SoC? Describe a means by which this problem can be addressed. (4 marks)

f) Why might production testing become increasingly challenging in future ASICs? (4 marks)