Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Implementing System-on-Chip Designs

Date: Wednesday 20th May 2015
Time: 14:00 - 16:00

Please answer Question 1 and also TWO other questions from the remaining FOUR Questions provided

This is a CLOSED book examination

The use of electronic calculators is NOT permitted
Section A

This question is compulsory.
Answer any ten of the subsections.
Each subsection carries two marks.

1. a) You have a logic synthesis tool which cannot cope with a multiplication operator and you need to multiply a value by 1280. Express this as a combinatorial Verilog statement. (2 marks)

b) Briefly explain what is meant by a “H-tree”, including what this might be used for and why it helps in an SoC context. (2 marks)

c) Test patterns are used during both the design and manufacturing phases of SoC production. How might sets of these patterns differ? (2 marks)

d) In figure 1 each PMOS transistor has a width of $10\lambda$. Estimate the width of the NMOS transistors to give the gate roughly equal output rise- and fall-times. Give a brief statement of your reasoning. (2 marks)

![Figure 1:](image)

e) Verilog allows the definition of absolute delays when modelling hardware but the ASIC synthesizer will strip these out. Why does it do this? (2 marks)

f) Serial access to the extensive state in an SoC is quite slow. Why, then, does the JTAG standard use serial access for test, debugging and, sometimes, configuration purposes? (2 marks)

g) Briefly explain what is meant by:

(i) Clock skew
(ii) Clock jitter (2 marks)
h) Bidirectional buses – where data can travel in different directions along wires – are sometimes used between chips on a PCB. Why is this done? Why are they rarely, if ever, now used in the ‘core’ of an SoC? (2 marks)

i) On a VLSI SoC, explain what is meant by:

   (i) Transistor threshold
   (ii) Gate threshold (2 marks)

j) Verilog has two ‘compare for equality’ operators: ‘==’ and ‘===’. What is the difference between them? (2 marks)

k) Figure 2 shows a symbol for a complex gate which will be implemented as a single stage of CMOS logic. How many transistors does it require? (2 marks)

   ![Figure 2: A2OI complex gate](image)

l) Why are the properties of state-of-the-art VLSI CMOS transistors today harder to predict than they were 20 years ago? (2 marks)
Section B

Answer any two questions from this section.

2. a) Explain what a ‘frame store’ is and how it is addressed. (4 marks)

b) A medium resolution graphics display has a resolution of $1280 \times 720$ pixels, displays $2^{16}$ colours and refreshes the screen at 50 Hz. Estimate the frame store bandwidth required to keep the display screen stable. (Exact arithmetic is not required; a reasonably close approximation is acceptable. You must indicate the units, however.) (2 marks)

c) The display above is used in a hand-held video-games console which must be able to run real-time, frame-rate ‘Shoot-’em-up’ games using full-screen resolution. What is the minimum additional frame store bandwidth requirement? (2 marks)

d) Why is it likely (and, probably convenient) that somewhat more than the minimum bandwidth already calculated would be desirable? (2 marks)

e) The frame store is to be made of RAM with a cycle time of 25 ns. (This RAM has a constant access time regardless of the address pattern.) Suggest how you might architect the framestore to meet the system requirements. (6 marks)

f) The original design required a single-chip SoC using a conventional microprocessor, licensed from a third party, for the graphics drawing. A team member suggests developing an in-house graphics accelerator instead. Briefly discuss the advantages and disadvantages to adopting this suggestion. (4 marks)
3. a) Give two distinct reasons why energy efficiency is a major consideration in SoC design. (2 marks)

b) Why might different logic blocks of an SoC use different supply voltages? (2 marks)

c) (i) What is meant by ‘Dynamic Voltage and Frequency Scaling’ (DVFS)?
(ii) What benefit(s) does it confer?
(iii) Describe the sequence of operations used when DVFS is applied. (6 marks)

d) When crossing between different supply domains, explain why it is not sensible to wire a logic signal sourced from a subcircuit with low supply voltage directly into a gate supplied at a higher voltage. Assume the ‘grounds’ (Vss) are at the same potential. (4 marks)

e) Figure 3 shows a circuit which interfaces a logic signal between two different voltage domains. Explain how it works, clearly describing the possible voltage levels at the various points, both signals and supplies. (Reproducing the figure and labelling may help you with this.) (6 marks)

Figure 3: Level shifter
4. a) As Systems on Chip increase in complexity – particularly in the number of processor subsystems – there is a move from ‘traditional’ bus-based architectures towards Network-on-Chip (Noc). Why is this? (2 marks)

AXI is used as a high-performance standard for on-chip interconnection. It comprises several semi-independent, unidirectional pipelines between macro-blocks on a chip. It is used for purposes such as connecting networks to DMA peripherals or SDRAM to a processor’s cache.

b) Why is this fast, pipelined architecture reasonably well suited to this type of task? (2 marks)

AXI is synchronous; items {commands, addresses, data} all move between stages on the same clock. Flow control is local. Part of a pipeline is shown in figure 4.

- Valid indicates a stage contains a data item
- Ready indicates a stage may receive a data item

An item moves to the next stage if the corresponding control signals indicate valid and ready in the same cycle, and not otherwise. For performance purposes it is desirable to allow all stages to contain valid items and pass these on on every clock.

![Figure 4: AXI pipeline stages](image)

Figure 4: AXI pipeline stages

c) Why is it expedient to use localised control rather than attempt to stall the transfer ‘globally’ on a given link? (2 marks)

*Note: in the following parts of this question, the ‘data’ and any associated latches may be neglected. Only the control signals are of interest.*

d) The ‘local’ flow control has implications for the function of each stage. Sketch the state diagram for the central logic stage in figure 4 showing its transitions for all input combinations assuming the stage is capable of transferring a data item on every clock under ideal conditions but can be stalled arbitrarily by its inputs. Annotate the figure with the state of the output signals in each state. (8 marks)

e) Derive a Verilog description of the stage described above. Do not include the data buses. (Minor syntactic mistakes will not be penalised.) (6 marks)
5. a) When implementing an algorithm as a synchronous circuit a functional RTL is usually produced. What indication of the ultimate performance can be derived by simulating this? (2 marks)

b) After the initial synthesis of an RTL, how might the cycle time be estimated? (2 marks)

c) Why is the cycle time estimate likely to increase when the synthesised netlist is Placed & Routed? (2 marks)

d) An ASIC for a data-streaming application is being designed. After a trial place-and-route, simulation indicates that the initial RTL model can only achieve just over half its required throughput. Suggest two different possible approaches the RTL author could attempt to reach the desired speed. In each case briefly mention any advantages and disadvantages to the approach. (8 marks)

e) After applying a method from the preceding part of the question, the resynthesised design achieves about 95% of the necessary throughput. This can be improved to meet the target by applying constraints to the synthesiser. What techniques can this CAD tool use to improve the cycle time? (6 marks)