Q1: Attempted by 20/23
Generally good answers for parts a)-c); answers weak on interrupt details in parts d)-f). Common Errors included overlooking the role of IRQ enable at the start, and weak understanding of the requirements for re-entrant IRQ handling [part f].

Q2: Attempted by 18/23
Generally OK on parts a)-d), though some very waffly answers. Few good answers to parts e) despite this being exactly the issue covered by the last major coursework deliverable.

Q3: Attempted by 12/23
Answers here were mainly either very good or very poor! Good answers were from those who clearly knew how many address bits were needed for what cache function, and poor answers from those who didn't. As the question specifically asked for precision in indicating the use of address lines it is surprising that those who did badly chose this question.

Q4: Attempted by 12/23
As with Q3, a rather bimodal set of marks. Only a few candidates really got to grips with part d), which required little more than seeing that without a TLB each data transfer requires 3 memory access, with a TLB this goes down (almost) to 1, so the TLB gives a 3x speed-up.

Q5: Attempted by 7/23
In contrast to Q3 & Q4, most answers to this question got middling marks in the 50% to 65% range. Answers to part b) showed evidence of memorisation - the example is similar to, though not the same as, the one in the book and on-line material, and a common feature was the appearance of a Timer module that the question doesn't ask for (but is in the book)!