Disappointing exam results (on average) this year, although the spread was very wide. The exam was slightly different due to policy changes on the removal of options on questions; stylistically, though, it was substantially the same as in previous years and an attempt to 'broaden' the questions to compensate for the lack of choice was made in setting the paper.

Overall there was evidence that facts had often been understood but not interpreted and applied appropriately to the questions asked. It is not clear as to whether this is 'not reading the question properly' or an inability to extrapolate from what is known. This is a third year module and some interpretation should be expected at this level.

Without commenting on every section of the paper, here are some particular issues:

Q.1(b) Maybe this is a bit of a 'trick' but the (mis)behaviour of Verilog has been emphasised repeatedly. The outcome here is not defined; maybe over half the candidates failed to realise this.

Q.2 Generally well answered although some candidates had problems thinking about/describing architectural choices early on. Most seemed to relish the later, implementational sections of the question.

Q.3 The circuit level details, particularly the different lengths of logic paths, was under-appreciated. Leakage seems to be understood implications. Overall, the average was a bit low on this question.

The practical work in the module largely succeeded (eventually) although the time management was clearly an issue for nearly everybody. It seems to have been a positive experience ... in the end.