The average mark was approximately 60% including one “outlier” very low scoring script. Half of the papers achieved a mark of over 60%. Answers to questions 3 had, on average, slightly lower marks than either of questions 1 and 2.

Some of the key points where marks were lost included:

For Question 1b, comparing parallel hardware and related programming models, a number of students gave weak answers to the issues involved in implementing each programming model (Data Sharing and Message Passing) on each type of hardware (Shared Memory, Distributed Memory).

For Question 2d/2e (Transactional Memory - Versioning/Validation) a number of students were confused between versioning and validation.

For Question 2f some students failed to relate the mechanism and state saved during the use of LDL/STC to a transaction, so did not explain why LDL/STC can be considered to implement a transaction.

For Question 3a (Explain Cache Coherence), there were several rather basic answers that, for example, did not discuss different models of consistency (e.g. sequential consistence and release consistency).

For part 3c, several answers failed to correctly identify and name the “Owner” state.

For part 3f, most answers did not explain that with sequential consistency the equivalent sequential execution arises from any arbitrary interleaving of instructions or methods (in which instructions/methods appear in program order for each thread).

In part 3g, several answers did not clearly explain the relation between release consistency and out-of-order execution.