

# UG Exam Performance Feedback

## Third Year

### 2018/2019 Semester 1

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COMP32211 Implementing System-on-Chip Designs

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**Comments** In the main the exam was well answered and the results profile looks satisfactory, which suggests it was fair.

As always, Q1 (short questions, often bookwork) produced higher average marks than the longer questions with more problem elements: this is expected and intended.

A complete part-by-part breakdown seems superfluous. Only particular issues are highlighted.

Q1 - pleasing that topics like 'regression testing' are now clearly understood, presumably as a result of the revised software engineering module. This has not always been the case.

The differences in production test and design verification are poorly understood though. If not memorised, these should be deducible if their purposes and the sources of potential problems are comprehended. This is somewhat worrying.

Q2 - the complex gate problem (a) was generally solved well although there were a few failures to 'sanity check' answers. The transistor sizing issue (b) was reasonably well done, but more people were baffled and a number hadn't understood (or read) the question completely. Some of the implications of wire length were appreciated although many spotted speed but neglected the power issue; this was deliberate in the question setting. Despite the 'hint' from (c), most neglected the opportunities for the CAD to use bigger transistors for more drive. The final problem (f) is deliberately open with no exact answer.

Most candidates spotted the major implications and had some potential solutions; few candidates provided enough to approach a 'full' mark but this was intended in the question setting.

Q3 - clearly much (but not all) based around the practical work and experience.

The 'big' problem (e) has a couple of common types of -functional- error; answers were disappointing in a few instances but generally appear fair. A few candidates 'complained'/wanted to have the whole function in Verilog, but having 4-bit counters composed into a larger design is -not- a fault. (The intention was to cross the schematic/HDL boundaries; there is a hint that the schematic may be faulty - the fault can be cured in the HDL module itself but a confident candidate could explain this.)

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