The average mark was approximately 68%. Answers to questions 2 had, on average, slightly higher marks than either of questions 1 and 2.

Some of the key points where marks were lost included:

For Question 1b, some students did not have a clear grasp of Host-GPU architecture and so were unable to discuss relationship to the data sharing/message passing models.

For Question 1c, some students were confused over the precise meaning of dynamic scheduling and/or the implication of the work distribution (for example, the implications of the cost of isSquare() vs procA()).

For Question 16, many students (but by no means all) did not point out that test-and-set has the opposite semantics to the traditional semaphore.

For Question 2 was very well answered by a large number of students (a little too easy?). The biggest issue was that many students were not clear that register operations do not affect the state of cache lines and there was some confusion over when the difference M state and E states.

For part 3f(i), not all students were clear that speculation is automatic (just requiring a compiler flag) whereas TM requires annotations in the code.

For part 3f(ii), the biggest problem was the lack of clarity and precision in explaining the extra resources each technique requires.