

UG Exam Performance Feedback

Third Year

2019/2020 Semester 1

COMP32211 Implementing System-on-Chip Designs

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Comments The results were, in the main, good with some very high marks although there were also a few scripts which were disappointing.

Q.1 - short unconnected questions covering the breadth of the course - was generally well answered although there were some parts which caused problems for many candidates. Notably, here, the transistor structure of a complex gate baffled many and a scan chain is more than just "a wire". The question on choosing a multiplier for a filter typically would have been better answered if it had been read properly: it first asked for what factors might influence design choice before making an appropriate suggestion as to a choice; this former (easier?) part was often neglected. Parts more closely related to the practicals were generally well understood, sometimes with some stumbling on terminology which was not penalised as long as the intent was clear.

Q.2 started with more lab-based material but took things deeper: '===' is clearly only half-understood by some. The verification aspects were well covered. One omission, connected with delaying output changes in the examples, is that by moving the effect of the assignment later it guarantees that it cannot affect any other operations at the (critical) clock edge.

The later part of this question morphed into more 'lecture' material which was usually well covered.

Q.3 is more open; it sets a context and poses a design problem to which there is no single 'right' answer. As might be expected, this question was the one where a number of candidates were, at least partially, caught out. Particularly worth mention was that many failed to take into account the factor of 4 between the RAM block sizes (32-bit words) and the requirement (in bytes); these are clear in the paper. Usually the same candidates did account for these sizes in the throughput. Some credit was given for method and results which showed, appropriately, that one was twice the area of the other: this should have been very clear - not everyone had such answers though.

The later parts - intended to be increasingly challenging - were often better answered. More candidates than anticipated suggested interleaving blocks; there are easier ways of providing bandwidth such as simply widening the buses to the memory (since there are multiple blocks, build a buffer with a 64-bit word!) but this was remarkably unpopular. One general criticism of answers here is the clarity of the explanation; if, for example, a sketch diagram is useful don't hesitate to add such and don't wait to be asked. It should be clear why suggestions of simply increasing the clock frequency were not credited!
