A SHALLOW WATER MODEL ON AN HETEROGENEOUS ARM ARCHITECTURE

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By
Juncheng Li
Supervisors: Graham D. Riley, John R. Gurd
School of Computer Science
Abstract

Two previous MSc dissertations [Pap12, Tan13] have focused on parallelisation of a shallow water benchmark on various machines with homogeneous or heterogeneous architectures. The CPUs on these machines are usually X86 architecture, which is an implementation of complex instruction set computing architecture. In recent years, ARM processors, which are based on a reduced instruction set computing architecture have been a success in the mobile device market. ARMv7-A architecture CPUs now support multi-core, native floating point instructions, and single instruction multiple data instructions. Combined with powerful Mali GPUs, the resulting heterogeneous ARM architecture is becoming interesting for high performance computing.

The parallelisation research in this project has focused on the shallow water equations benchmark on an ARM Cortex-A15 dual core CPU and Mali-T604 GPU. Work with an OpenMP benchmark on the CPU has focused on the effects of the chunk size used for scheduling, loop fusion and data reuse. An OpenCL benchmark originally targeted at an NVIDIA GPU has been ported to the Mali-T604, and memory optimisation has been investigated. As the ARM architecture is aimed at having high power performance, the power performance of the shallow water benchmark has also been investigated.

The results show that even after optimisation, the shallow water benchmark does not perform well on the ARM Cortex-A15 CPU and Mali-T604 GPU compared with the multi-core and GPU architectures used in current HPC systems. However, it appears to achieve a competitive power performance compared with a traditional multi-core processor.

A number of execution behaviours that were not able to be fully explained due to time limitations were observed and these are left for future work.